Nature of Interface Traps in Ge MIS Structures with GeO₂ Interfacial Layers

N. Taoka1*, W. Mizubayashi1, Y. Morita1, S. Migita1, H. Ota1 and S. Takagi1,2
1MIRAI-NIRC, AIST Tsukuba West 7, 16-1, Onogawa, Tsukuba 305-8569, Japan
2The University of Tokyo, 7-3-1 Hongo, Bunkyo-ku, Tokyo 113-8656, Japan
*Present affiliation: The University of Tokyo, Phone:+81-3-5841-6733, E-mail: ntaoka@mosfet.t.u-tokyo.ac.jp

1. Introduction
A high mobility channel is still effective to gain a drive current of a short channel device[1]. Therefore, a Ge channel with high mobility is one of attractive candidates to overcome a limit of device scaling. The high performances of Ge p- and n-channel MISFETs with GeO₂ interfacial layers (IL) have already been demonstrated[2,3]. On the other hand, key parameters to enhance the performances have not been fully understood yet. Although interface trap density (Dit) is one of the key parameters, nature of Ge MIS interface traps is also important parameters influencing on the device performances.

In this study, we have systematically studied the interface traps in Ge MIS structures with GeO₂ IL grown at various temperatures. It is found that the natures of the Ge MIS interface traps depend on the oxidation temperatures, and that acceptor-like traps are widely distributed in Ge bandgap.

2. Experimental Procedure
The fabrication process flow of the capacitors and the resulting gate stack structures are shown in Fig. 1(a) and 1(b), respectively. After device isolation, Ge wafers were annealed at 420°C in O₂ ambient. Subsequently, a 10-nm-thick SiO₂ layer as a gate insulator film was deposited by LPCVD. The formation of a GeO₂ layer at the SiO₂/Ge interface have already confirmed by XPS measurement[4]. Successively, TaN and NiSi gate electrode were formed by sputtering and dry etching. Next, post metallization annealing (PMA) was carried out at various temperatures for some samples. C-V and conductance versus frequency measurements were carried out at various temperatures.

3. Results and Discussion
The 2-nm-thick GeO₂ IL was observed in the capacitor without PMA as shown in Fig. 2(a), while the thick GeO₂ IL was observed in the capacitor with PMA at 600°C as shown in Fig. 2(b) as reported ref[5]. The oxide capacitances of 1MHz C-V curves decrease with increasing the PMA temperatures as shown in Fig. 3. These results indicate that the Ge surfaces are oxidized during PMA. Energy distributions of Dit near the conduction band edge (CBE) of the capacitors with PMA at various temperatures are shown in Fig. 4. It is found that Dit decreases with an increase in the temperature range as well as the GeO₂/Ge interfaces formed by thermal oxidation[6]. The energy dependence of the standard deviation (σs) of surface potential fluctuation induced by interface charges is shown in Fig. 5. Also, the correlation between Dit and σs is shown in Fig. 6. It is clearly found that Dit increases with an increase in temperature opposite to the decrease of Dit with increasing temperatures. Furthermore, Dit in the case of the low PMA temperatures decrease toward CBE, suggesting that the charged centers decrease by capturing electrons. On the other hand, in the case of high PMA temperatures, Dit increase toward CBE. These complicated behaviors could be induced nature of fast and/or slow interface traps. Therefore, nature of Ge MIS interface traps is carefully investigated in the next paragraph.

The first-principles calculations revealed that interface traps formed by Ge dangling bonds have a unique nature, charge neutrality level of which is located near VBE[7]. The unique nature might lead to an asymmetric energy distribution of interface properties on lower and upper half of bandgap. For this reason, interface properties are also investigated in lower half of bandgap using p-type substrates. Figure 7 shows Vfb of the capacitors with p- and n-type substrates with PMA at 600°C as a function of measurement temperatures. It is clearly observed that the temperature dependence of Vfb in the case of the p-type substrate is larger than that of the n-type one. Figure 8 shows C-V curves of the capacitors with the p- and n-type substrates measured at 80K. The negative ΔVfb of the capacitor with the p-type substrate is much larger than that of the n-type case, where the work function of 4.4eV for TaN was used[8]. At the flatband bias condition, Eref is located at around -0.33 and 0.33eV for the p- and n-type substrates, respectively. Then, the difference of fixed oxide charge densities between p- and n-type cases is identical to 8×10¹⁵cm⁻². This indicates that positive interface charges decrease or negative interface charges increase when Eref moves from -0.33eV to 0.33eV. In order to judge the decrease of positive charges or the increase of the negative charges, σs is carefully investigated at various temperatures. Figure 9 shows the conductance curves measured at Eref=0.31 and 0.26eV at 80K. It is clearly observed that the broadening of the conductance curve measured at 0.26eV is much larger than that measured at -0.31eV. The energy distributions of σs measured at various temperatures are shown in Fig.10. Note that σs increases toward CBE from VBE, suggesting that charged center density increases capturing electrons. Therefore, these results suggest that acceptor-like traps are widely distributed in Ge bandgap.

Figure 11 shows energy distributions of Dit evaluated by the conductance method. The interface traps are symmetrically distributed to midgap as well as the GeO₂/Ge interfaces formed by thermal oxidation[6]. In this case, the integrated interface trap density (Nt) from -0.33 to 0.33eV is approximately 3×10¹⁵cm⁻². Even if all the interface traps are negatively charged, the large Vfb shift as shown in Fig. 8 can not be explained. This imply that a large number of acceptor-like slow traps exist at the GeO₂/Ge interface because the ac response associated with the slow traps does not contributes to the peak of conductance curves, while the charged slow traps induce Vfb shifts.

4. Conclusions
The Ge MIS interface traps formed at low temperature have donor-like nature, while those formed at high temperature have acceptor-like nature near CBE. In addition, it is found that the acceptor-like traps are widely distributed in Ge bandgap at the interface formed at high temperatures.

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References
Positive fixed oxide charges

Negative charged traps

Compensation of negative V FB shift due to negative charged traps

Neutral traps

Negative V FB shift due to positive fixed oxide charges

ESF and E i are Fermi level at a Ge surface, intrinsic Fermi level of Ge, respectively.

Here, ESF-E i is represented in the unit of kT/q, where k, T and q are the Boltzmann’s constant, the absolute temperature, the elementary charge, respectively.

D it and σ s were evaluated at ESF-E i = 0.26 eV.

Nit = 3x10 11 cm 2

0.33 eV

Fig. 10: Energy distributions of σ s measured at various temperatures.

Fig. 11: Energy distributions of D it for the capacitor with PMA at 600°C evaluated from the conductance method.

Fig. 12: Schematic diagram of the relationship between the location of interface charges and the nature of interface traps for (a) p-type and (b) n-type substrates at 80K.