Extended Abstracts of the 2010 International Conference on Solid State Devices and Materials, Tokyo, 2010, pp27-28

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Nature of Interface Traps in Ge MIS Structures with GeO_2 Interfacial Layers

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1. Introduction

A high mobility channel is still effective to gain a drive current of a short channel device[1]. Therefore, a Ge channel with high mobility is one of attractive candidates to overcome a limit of device scaling. The high performances of Ge p- and n-channel MISFETs with GeO_2 interfacial layers (IL) have already been demonstrated[2,3]. On the other hand, key parameters to enhance the performances have not been fully understood yet. Although interface trap density (D_{it}) is one of the key parameters, nature of Ge MIS interface traps is also important parameters influencing on the device performances.

In this study, we have systematically studied the interface traps in Ge MIS structures with GeO_2 IL grown at various temperatures. It is found that the natures of the Ge MIS interface traps depend on the oxidation temperatures, and that acceptor-like traps are widely distributed in Ge bandgap.

2. Experimental Procedure

The fabrication process flow of the capacitors and the resulting gate stack structures are shown in Fig. 1(a) and 1(b), respectively. After device isolation, Ge wafers were annealed at 420°C in O_2 ambient. Subsequently, a 10-nm-thick SiO_2 layer as a gate insulator film was deposited by LPCVD. The formation of a GeO_2 layer at the SiO_2/Ge interface have already confirmed by XPS measurement[4]. Successively, TaN and NiSi gate electrode were formed by sputtering and dry etching. Next, post metallization annealing (PMA) was carried out at various temperatures for some samples. C-V and conductance versus frequency measurements were carried out at various temperatures.

3. Results and Discussion

The 2-nm-thick GeO_2 IL was observed in the capacitor without PMA as shown in Fig. 2(a), while the thick GeO_2 IL was observed in the capacitor with PMA at 600°C as shown in Fig. 2(b) as reported ref[5]. The oxide capacitances of 1MHz C-V curves decrease with increasing the PMA temperatures as shown in Fig. 3. These results indicate that the Ge surfaces are oxidized during PMA. Energy distributions of D_{it} near the conduction band edge (CBE) of the capacitors with PMA at various temperatures are shown in Fig. 4. It is found that D_{it} decreases with an increase in the temperature range as well as the GeO_2/Ge interfaces formed by thermal oxidation[6]. The energy dependence of the standard deviation (σ_s) of surface potential fluctuation induced by interface charges is shown in Fig. 5. Also, the correlation between D_{it} and σ_s is shown in Fig. 6. It is clearly found that σ_s increases with an increase in temperature in spite of the decrease of D_{it} with increasing temperatures. Furthermore, σ_s in the case of the low PMA temperatures decrease toward CBE, suggesting that the charged centers decrease by capturing electrons. On the other hand, in the case of high PMA temperatures, σ_s increase toward CBE. These complicated behaviors could be induce nature of fast and/or slow interface traps. Therefore, nature of Ge MIS interface traps is carefully investigated in the next paragraph.

The first-principles calculations revealed that interface traps formed by Ge dangling bonds have a unique nature, charge neutrality level of which is located near VBE[7]. The unique nature might lead to an asymmetric energy distribution of interface properties on lower and upper half of bandgap. For this reason, interface properties are also investigated in lower half of bandgap using p-type substrates. Figure 7 shows V_{FB} of the capacitors with p- and n-type substrates with PMA at 600°C as a function of measurement temperatures. It is clearly observed that the temperature dependence of V_{FB} in the case of the p-type substrate is larger than that of the n-type one. Figure 8 shows C-V curves of the capacitors with the p- and n-type substrates measured at 80K. The negative ΔV_{FB} of the capacitor with the p-type substrate is much larger than that of the n-type case, where the work function of 4.4eV for TaN was used[8]. At the flatband bias condition, E_{SF} are located at around -0.33 and 0.33eV for the p- and n-type substrates, respectively. Then, the difference of fixed oxide charge densities between p- and n-type cases is identical to $8\times10^{11}cm^{-2}$. This indicates that positive interface charges decrease or negative interface charges increase when E_{SF} moves from -0.33eV to 0.33eV. In order to judge the decrease of positive charges or the increase of the negative charges, σ_s is carefully investigated at various temperatures. Figure 9 shows the conductance curves measured at E_{SF}-E_i=-0.31 and 0.26eV at 80K. It is clearly observed that the broadening of the conductance curve measured at 0.26eV is much larger than that measured at -0.31eV. The energy distributions of σ_s measured at various temperatures are shown in Fig.10. Note that σ_s increases toward CBE from VBE, suggesting that charged center density increases capturing electrons. Therefore, these results suggest that accepter-like traps are widely distributed in Ge bandgap.

Figure 11 shows energy distributions of D_{it} evaluated by the conductance method. The interface traps are symmetrically distributed to midgap as well as the GeO_2/Ge interfaces formed by thermal oxidation[6]. In this case, the integrated interface trap density (N_{it}) from -0.33 to 0.33eV is approximately $3\times10^{11}cm^{-2}$. Even if all the interface traps are negatively charged, the large V_{FB} shift as shown in Fig. 8 can not be explained. This imply that a large number of acceptor-like slow traps exist at the GeO_2/Ge interface because the ac response associated with the slow traps does not contributes to the peak of conductance curves, while the charged slow traps induce V_{FB} shifts.

Schematic diagrams of relationship between the locations of interface charges and the nature of interface traps are shown in Fig. 12. In Fig. 12(a), the neutral fast and slow interface traps are located above E_F. Then, the V_{FB} shifts are dominantly induced by the fixed oxide charges. On the other hand, in Fig. 12(b), the fast and slow interface traps are negatively charged by capturing electrons. Therefore, the V_{FB} shifts due to the fixed oxide charges are compensated by the contribution of negative charges.

4. Conclusions

The Ge MIS interface traps formed at low temperature have donor-like nature, while those formed at high temperature have acceptor-like nature near CBE. In addition, it is found that the acceptor-like traps are widely distributed in Ge bandgap at the interface formed at high temperatures.

Acknowledgements This work was supported by NEDO. Technical support by NPRT of NIRC, AIST.

References [1]A. Lochtefeld *et al.*, EDL, **22**, 591(2001). [2]Y. Nakakita *et al.*, IEDM, 877(2008). [3]K. Morii *et al.*, IEDM, 681(2009). [4]N. Taoka *et al.*, Semicond. Sci. Technol. **22** (2007) S114. [5]N. Taoka *et al.*, JJAP, **49**, 04DA09(2010). [6]H. Matsubara *et al.*, APL, **93**(2008) 032104. [7]P. Broqvist *et al.*, PRB, **78** 075203(2008). [8]Y. Kamimuta *et al.*, IEDM, 341 (2007).

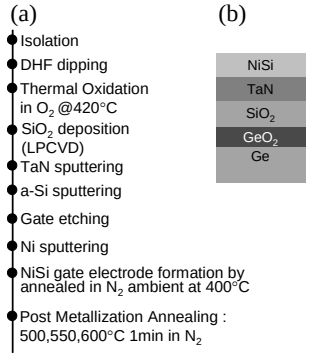

Fig. 1 (a) Fabrication process flow of the capacitors and (b) the gate stack structures of the fabricated capacitors.

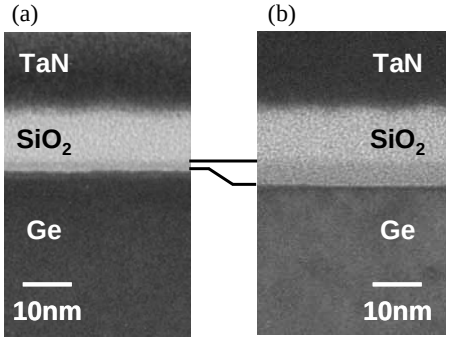

Fig. 2: TEM images of the fabricated capacitors (a) without and (b) with PMA at 600°C.

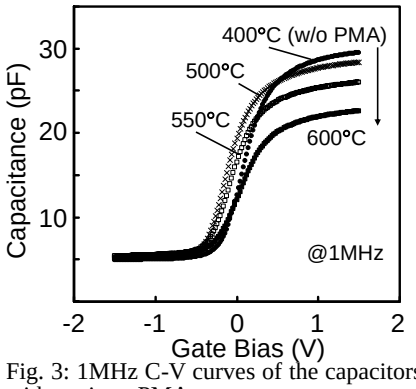

Fig. 3: 1MHz C-V curves of the capacitors with various PMA temperatures measured at room temperature.

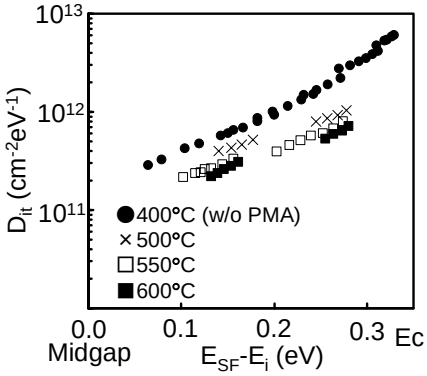

Fig. 4: Energy distributions of D_{it} for the capacitors with various PMA temperatures. Here, E_{SF} and E_i are Fermi level at a Ge surface, intrinsic Fermi level of Ge, respectively.

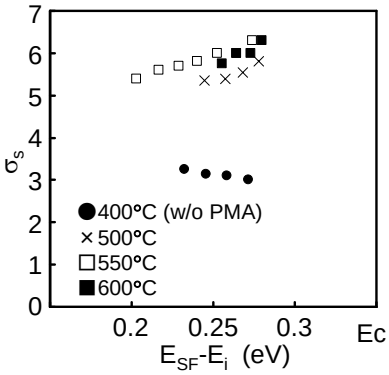

Fig. 5: Energy distributions of σ_s for the capacitors with various PMA temperatures. Here, σ_s is represented in the unit of kT/q, where k, T and q are the Boltzmann's constant, the absolute temperature, the elementary charge, respectively.

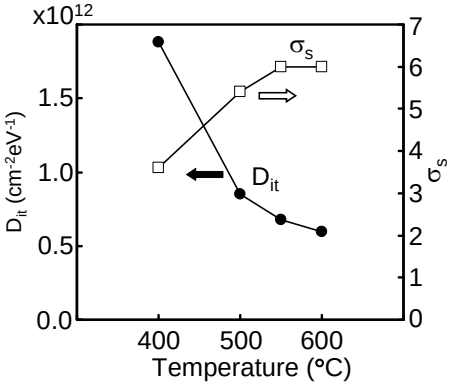

Fig. 6: PMA temperature dependence of D_{it} and σ_s. D_{it} and σ_s were evaluated at E_{SF}-E_i=0.26eV.

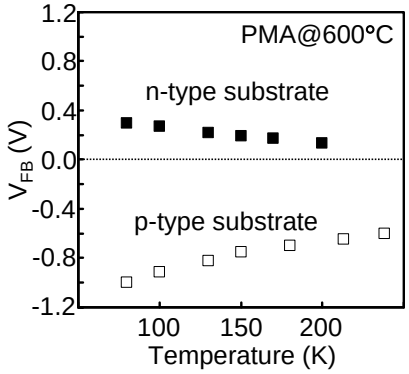

Fig. 7: Dependence of V_{FB} on measurement temperature for the capacitor with PMA at 600°C.

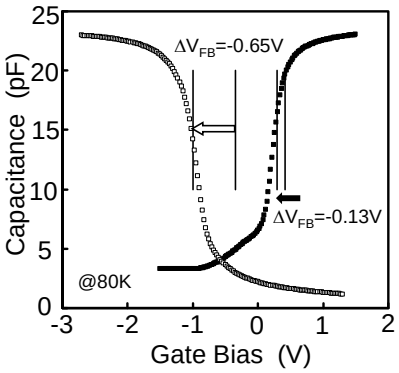

Fig. 8: 1MHz C-V curves of the capacitors with p- and n-type substrates measure at 80K.

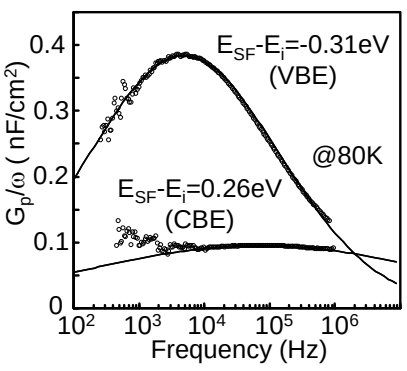

Fig. 9: Conductance curves measured at near CBE and VBE.

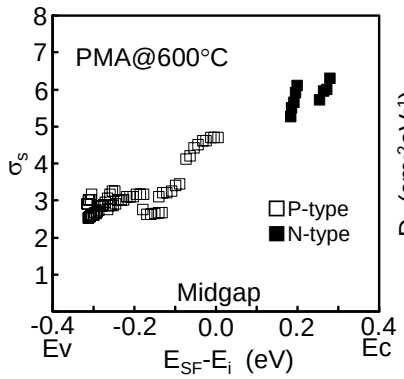

Fig. 10: Energy distributions of σ_s measured at various temperatures.

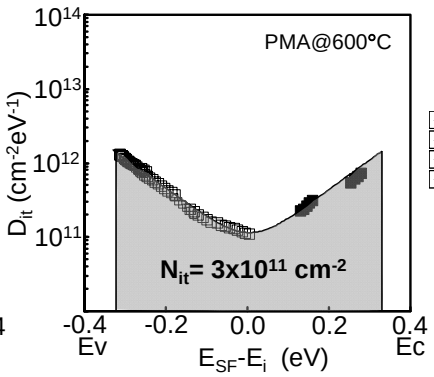

Fig. 11: Energy distributions of D_{it} for the capacitor with PMA at 600°C evaluated from the conductance method.

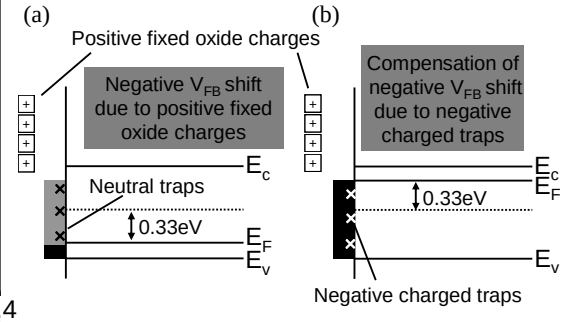

Fig. 12: Schematic diagram of the relationship between the location of interface charges and the nature of interface traps for (a) p-type and (b) n-type substrates at 80K.