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Fermi-level Pinning and NBTI Free of CMOS HfO_2 by Pre-CF_4 Plasma Passivation

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Abstract

In this paper, we demonstrate MG/Fluorinated HfO_2 CMOS device, focusing on interfacial reaction suppression by fluorine passivation at bottom HfO_2 interfaces. "Zero" interfacial layer forms in CMOS compatible gate first fabrication. 48% and 45% driving current enhancement were achieved for nFET and pFET respectively. The interfacial reaction between HfO_2 and Si substrate which caused Fermi-level pinning of MG/HK was sufficiently suppressed due to fluorine passivation of the Si substrate and the blocking of oxygen diffusion into the Si. In addition, a new physical model of fluorine re-incorporation was proposed to explain the NBTI characterization for pre-treated device.

Introduction

Although HfO_2 gate dielectrics are considered to be the most promising high-k dielectrics to meet the future ULSI application, it still remains some critical obstacles for integration of high-k/metal gate, such as Fermi-level pinning (FLP) effect and NBTI characteristics. Recently, fluorine (F) incorporation into the high-k gate dielectric has been shown to improve device performance and reliability [1]-[3]. In this paper, a CMOS compatible CF_4 plasma treatment technology is demonstrated. Material science, performance enhancement and reliability improvement for the pre-CF_4 plasma treated CMOS HfO_2 are deeply proposed.

Device Fabrication

A MG/HK gate stack were fabricated with CF_4 plasma treatment by PECVD. HfO_2 thin film was deposited on a HF-last Si surface by PVD (RF-sputter) system. Before HfO_2 thin film deposition, CF_4 plasma was used to treat the Si-wafer (denoted as pre-treat). And the other samples without any CF_4 plasma treatment before and after the hafnium dioxide deposition are denoted as as-dep.. TiN gate was then deposited also by RF-sputter for use as the gate electrode.

Results and Discussion

Figure 1(a) shows TEM images of HfO_2 thin film, which tended to have interfacial layers (IL) like Hf-silicate at the HfO_2/Si interfaces. During the film growth and post-processing, the formation of an interfacial SiO_2-like IL limits the reduction of the effective oxide thickness (EOT). However, the IL was effectively suppressed for the pre-treat sample (Fig.1(b)).

In Fig.2., for the as-dep. sample, one observes a strong and sharp band at 1221 cm^{-1} from the Si-O_x surface layer on Si. The peak is very typical of the native oxide on silicon. After CF_4 plasma treatment, the native oxide band at 1221 cm^{-1} has disappeared and been replaced by a significantly weaker absorption band centered near 1180 cm^{-1} which is similar to that observed for amorphous SiO_2 films on Si [4]. It is believed that the reduction of native oxide re-growth on CF_4 plasma treated Si substrates resulted from the fluorine passivation of the silicon surface. From these results, it seems reasonable that for the as-deposited sample the excess oxidizing species such as oxygen radicals, ions, and molecules in the plasma diffuse into the silicon substrate and contribute to the interfacial layer growth. On the other hand, it is believed that the growth of interfacial layer is inhibited by fluorine passivation of the Si substrate and the blocking of oxygen diffusion into the Si [5]. This hypothesis is supported by both the TEM imaging and FTIR spectroscopy.

From SIMS analysis (Fig.3.), it is apparent that fluorine atoms have accumulated mainly at the interface between the HfO_2 thin film and the Si substrate after the CF_4 plasma pre-treatment. This observation indicated that fluorine atoms first are distributed at the surface of the silicon substrate after the CF_4 plasma pre-treatment, and then are incorporated into the HfO_2 thin film during the hafnium dioxide deposition to form fluorinated HfO_2 gate dielectrics. In addition, these fluorine atoms also terminate the dangling bonds of silicon substrate and accumulate at the interfacial layer region.

Fig.4. shows driving current has 48% and 45% increase for pre-CF_4 treated HfO_2 nFET and pFET, respectively. Besides, I_D-V_G transfer characteristics of the as-deposited and CF_4 pre-treated HfO_2 are also shown in the inset of Fig. 4. Decreased V_{TH} and I_{OFF} reduction can be observed for Fluorinated HfO_2 nFET. (W/L=100/10 μ m)

Fermi-level pinning free phenomenon

Figure 5 shows the C-V curves of as-dep. and CF_4 plasma pre-treated HfO_2 thin films. As discussed before, the IL of pre-treat samples was effectively suppressed. The EOT decreased from 4.6 to 3.3, 3.7 to 2.9, and 3.6 to 2.7 nm respectively, for the different deposited film thicknesses. To understand the effect of pre-treat HfO_2 in effective work function (EWF) of metal gate electrode, the V_{FB} versus EOT are plotted in Fig.6(b) and the corresponding EWF are summarized in Fig.6(a). A TiN/SiO_2 MOSCAP were fabricated to be extracted the TiN EWF as the bulk work function [6]. It is obviously that the EWF of pre-treat samples are quiet similar to the sample with TiN on silicon dioxides(~4.6eV), on the contrary, the as-dep. are different from the pre-treat samples. It is believed to the interfacial reaction [7], if the charge transfer occurs by generating oxygen vacancy, a dipole will form and change the EWF as illustrated in Fig.7(b). For the pre-treat sample, as we mentioned before, the interfacial reaction is sufficiently suppressed by F passivation of Si-sub. surface and the blocking of oxygen diffusion into the Si, therefore FLP does not occur.

NBTI characterization in CF_4 plasma pre-treatment

To further investigation in pre-treat HfO_2 device reliability, NBTI characterization is discussed in this section. For the as-dep. sample, conventional NBTI degradation can be observed as shown in Fig.8. and Fig.9(a). However, the pre-CF_4 treated sample shows quite different NBTI characterization, such as decreased V_{TH} and I_{OFF}, increased I_D and g_m during NBTI stress, as shown in Fig.8, Fig.9(b) and 9(c). As discussed before, the EOT of pre-CF_4 treated sample is much smaller than the other samples. However, the stress voltage is the same for all samples. Therefore, the stress electric field of pre-CF_4 treated sample is 1.3 times than that of the other samples. As a result, the hole energy is high enough to break the strong Si-F bond (5.73eV) and create an interface trap by releasing fluorine species at the IL/Si interface (Fig.10). In addition, the released F would re-incorporate into HfO_2 film, resulting in trapping level increase, as shown in Fig.11. Therefore, the NBTI characterization of CF_4 pre-treated sample is quite different from conventional NBTI phenomenon.

Conclusion

For the first time, a Z-IL CMOS HfO_2 with F incorporation and its material science have been successfully demonstrated. Much improvement in device performance and reliability like FLP, NBTI were also deeply proposed in this paper.

References

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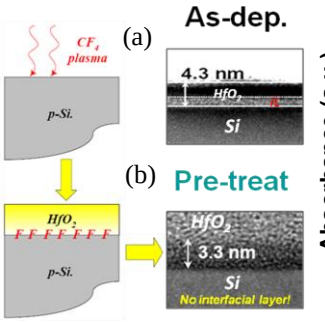

Fig. 1. TEM images of (a) as-dep. (b) pre-treat HfO_2 film.

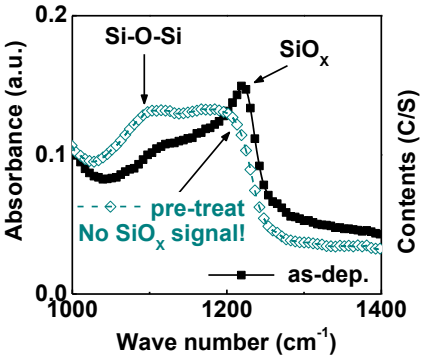

Fig.2. FTIR analysis for as-dep. and CF_4 pre-treat Si-wafers.

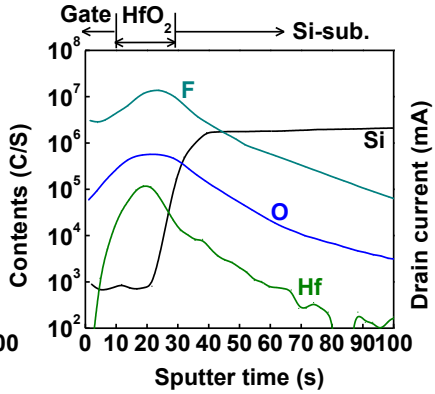

Fig.3. SIMS depth profile of MOS structure for fluorine oxygen, hafnium and silicon atoms distribution.

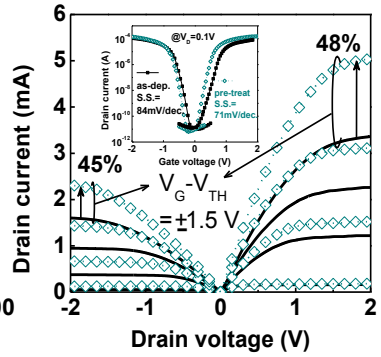

Fig.4. Enhanced drain current can be observed for nFET and pFET with pre-treat samples.

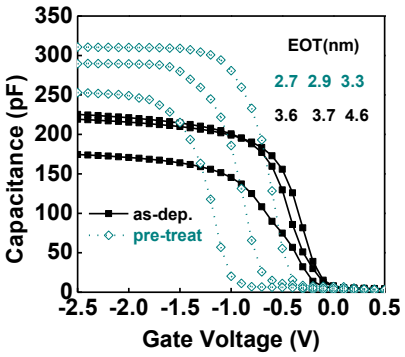

Fig.5. C-V curves of as-dep. and pre-treat samples. The EOT decreased from 4.6 to 3.3, 3.7 to 2.9, and 3.6 to 2.7 nm respectively, for the different deposited film thicknesses.

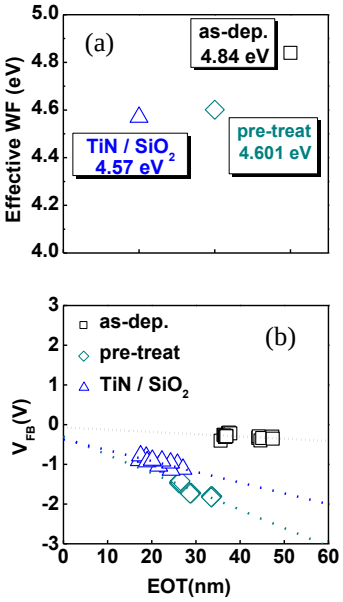

Fig.6. (a) EFW (b) V_{FB} vs EOT of all samples (TiN bulk work function are extracted from TiN/SiO_2)

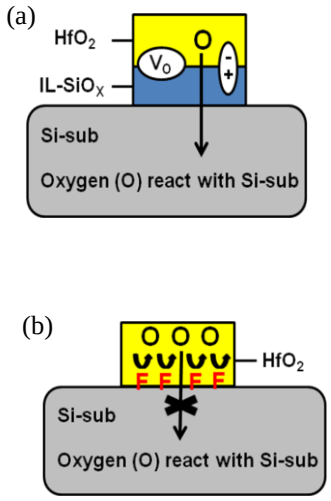

Fig.7. (a) Interfacial reaction model of FLP (b) illustration of release in FLP.

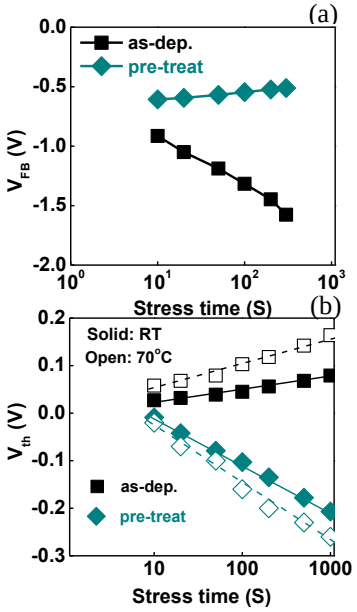

Fig.8. NBTI characteristics (@V_G-V_{th}=-1.5V) of all samples: (a)V_{FB} shift, (b) V_{th} shift

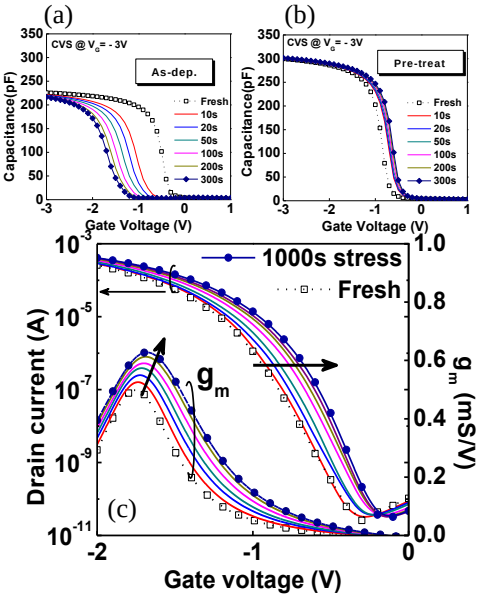

Fig.9. (a) as-dep. (b) pre-treat under CVS, (c) I_D-V_G and g_m curves (@70°C) of pre-CF_4 plasma treated sample during NBTI stress

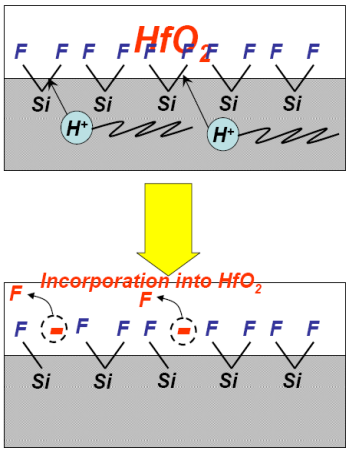

Fig.10. Physical NBTI model of CF_4 pre-treat HfO_2 dielectric. Si-F broken results in Vth decrease during NBTI stress.

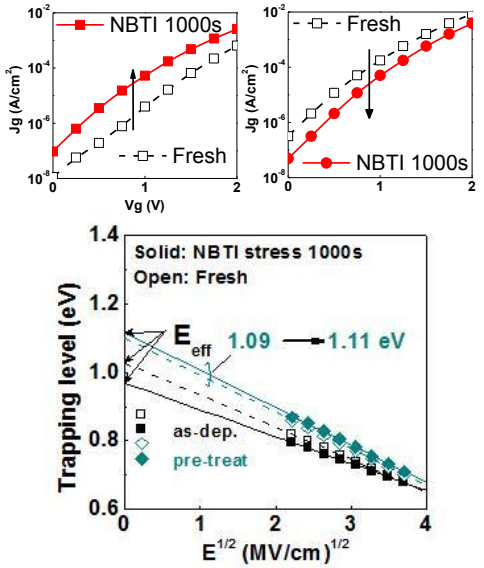

Fig.11. Extracted F-P trapping level of pret-treat HfO_2 increased after NBTI stress 1000s (1.09→1.11 eV) due to F re-incorporation.