Extended Abstracts of the 2010 International Conference on Solid State Devices and Materials, Tokyo, 2010, pp673-674

# Enhanced Electrical Uniformity and Breakdown of Multi-Step Deposited and Annealed HfSiO – Insight by Scanning Tunneling Microscopy

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## 1. Introduction

Structural defects in the thin high-κ dielectric can severely compromise the gate stack electrical characteristics[1]. In particular, grain boundaries (GBs) in the crystallized dielectric have been shown to present the localized high conductance paths[2], which increase voltage loading on the underlying interfacial oxide layer (IL), thereby accelerating the gate stack breakdown (BD)[3]. Mitigating the leakage through the high-k film is thus of primary importance for further gate stack scaling. In this work, we examine nanoscale electrical characteristics of HfSiO/IL gate stack formed by a two-step deposition and annealing process[4]. The results demonstrate that the two-step deposited high-k dielectric exhibits a (i) more amorphous-like structure; (ii) significantly narrower spread in the leakage current values; and (iii) strong retardation of the gate stack BD process, even by a localized stress over the GB regions compared to the conventional one-step process. An explanation suggests the leakage current is suppressed in the two-step samples due to a mismatch of the GBs in the two high-k layers[4].

## 2. Experimental Details

Two types of gate stacks with the ALD HfSiO (10% $SiO_2$) overlaying $SiO_2$ on the p-Si substrate were fabricated. One of the stacks was processed using a conventional continuous (one-step) high-k deposition followed by nitridation. For the other gate stack, a two-steps ALD process was performed. After the initial ~1-nm HfSiO deposition and nitridation, a second deposition and nitridation was performed to match the total thickness and nitride content of the one-step high-k film. Both samples were capped with the TiN film and exposed to a spike source/drain activation anneal. XPS revealed only subtle differences in the chemical composition of the two stacks (not shown). The high resolution cross-sectional TEM images confirmed almost identical HfSiO and interfacial layer (IL) thicknesses in both samples (Fig. 1). The metal layer was wet-etched away before scanning tunneling microscopy over the high-k surfaces was carried out in ultra-high vacuum (~$10^{-10}$ Torr) using a W tip. The bias voltage, $V_s$, was applied to the substrate. The spacing between the tip and high-κ surface was varied to keep the tunneling current constant during topography imaging. Local variations in the gate stack conductivity were examined by constant current tunneling spectroscopy; during these measurements, the feedback circuit was disabled allowing the *I-V* characteristics of the dielectric to be collected at the location of the tip by applying a voltage ramp. A set of the current values at a given bias collected at different points on the high-k dielectric surface forms a current map, depicting local conductivity variations over the scanned area.

## 3. Results and Discussion

### *A. Topography and Current Maps*

Fig. 2(a) and (b) show the topography image of the one-step and two-step HfSiO stacks, respectively. Coarse granular structures (denoted by the bright shades), averaging ~30 nm, are evident in the one-step HfSiO. However, the two-step sample exhibits much fine features indicating a more amorphous structure. Corresponding current maps are depicted in Fig. 2(c) and (d). Bright shades, arising from the "leaky" GBs surrounding regions of lower conductivity grains are apparent (see corresponding bright regions in Fig. 2(a)). These observations clearly show that thinner individual high-k layers in the multi-step stack suppress the formation of larger grains in the high-κ film[5].

### *B. Electrical Characteristics*

Tunneling current ($I_t$) spectra at GBs and grains (henceforth denoted as "GB-$I_t$" and "G-$I_t$" respectively) were extracted. In the one-step HfSiO stack (Fig. 3(a)), GB-$I_t$ is distinctly higher than G-$I_t$ (the current "plateau" in the negative regime is a result of the p-Si being in deep depletion, which limits $I_t$). In the two-step HfSiO, by contrast, GB-$I_t$ is only marginally higher than G-$I_t$ (Fig. 3(b)). Fig. 4 depicts the correlation between $I_t$ extracted under negative and positive $V_s$, which correspond to the electron injection from the substrate and tip, respectively. When $I_t$ is measured over the GBs in the tip-injection mode, the corresponding $I_t$ in substrate-injection mode is higher than the normal $I_t$ (whenever no GBs present in high-k film). This confirms the impact of high-κ quality on the underlying IL[2]. It is also apparent that $I_t$ taken over the GBs in the two-step HfSiO stack is much lower, indicating a larger effective tunneling barrier. On the other hand, $I_t$'s taken over grains are similar in both gate stacks. Fig. 5 shows cumulative distributions of $I_t$ normalized to that at the 63$^{rd}$ percentile. The steep "S"-type shape of the distribution of the leakage current values measured over the two-step HfSiO stack points to its better electrical uniformity.

### *C. Susceptibility to Stress-induced Degradation*

Since breakdown (BD) is controlled by the "weakest link" in the bi-layer high-κ gate stack[6], the time-to-breakdown, $T_{BD}$, of both gate stacks was evaluated by locally stressing 25 GBs (in each gate stack) at a constant voltage of 4 V. Both gate stacks exhibit progressive BD behavior indicating that the thin IL rather than a much thicker high-κ film controls the final BD[6] (Fig. 6). Even more importantly, $T_{BD}$ values measured at GBs in the one-step HfSiO are distinctly lower than those of the two-step HfSiO: 80% of the $T_{BD}$ data points taken at GBs in the one-step HfSiO stack fall within the range of 0-800 s while 90% of the $T_{BD}$ values taken at GBs in the two-step HfSiO fall in between 700-1200 s. This implies that the IL underlying the GBs in the one-step HfSiO stack generally wears out faster than that in the two-step HfSiO. This inference is also borne out in Fig. 7(a), which compares the spread in $I_t$, under the substrate injection mode (most sensitive to the trap generation in the IL[7]), taken during the 1$^{st}$ and 4$^{th}$ topography scan of a given area. A more substantial increase in the average $I_t$ as well as its spread following successive scans is evident for the one-step HfSiO stack. This feature is consistent with the less robust quality of the high-κ film in the one-step HfSiO stack as can be seen in Fig. 7(b). For comparison, stressing over the "bulk" of the grains was also carried out. Despite being stressed at a higher voltage (6 V), $T_{BD}$ values at the grain sites are much higher and similar in both type of stacks. In addition, the extensive progressive BD feature, which was evident when stress was performed at GBs, is clearly being suppressed in this case.

### *D. Misaligned GBs in the Two-Step HfSiO*

A qualitative explanation of the improved electrical uniformity and breakdown characteristics in the two-step HfSiO stack is provided in Fig. 8 and 9. Smaller grain sizes in the multi-step high-k deposited stacks (c.f. Fig. 2(a)) reduce the probability of a single GB propagating through the entire high-κ dielectric film (Fig. 8(a)), thus suppressing a highly conductive path through the high-k (Fig. 8(b)). Electrically, an "intact" high-κ (in either the upper or lower layer) translates into an additional tunneling barrier (Fig. 9(b) and (c), which reduces the likelihood of stress-induced breakdown as in the one-step stack (Fig. 9(a)).

## 4. Summary

The STM-measured topography and electrical characteristics of the HfSiO/IL gate stack formed using a one-step and two-step deposited high-k film are compared. The two-step high-k stack clearly shows improvements in its electrical uniformity and breakdown characteristics, which are ascribed to a mismatch in the GBs in the two high-k layers. This study indicates that a multi-step deposition and annealing process is a promising method for substantially improving the reliability of gate-first high-κ stacks.

**References** [1] McGilvery *et al.*, Springer Proc. in Phys (120), 325-328 (2008); [2] Yew *et al.*, SSDM 2009, 314-315; [3] Bersuker *et al.*, IRPS 2010, 373-378; [4] G. Bersuker et al., SSDM 2010; [5] Navrotsky *et al.*, J. Mater. Chem. (15), 1883-1890 (2005); [6] Bersuker *et al.*, IEDM 2008, 1-4; [7] Ong *et al.*, APL (92), 022904 (2008).

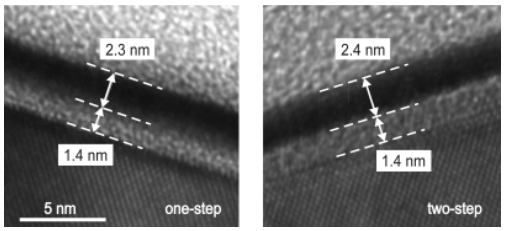


**Fig. 1** High resolution cross-sectional transmission electron micrographs showing similar HfSiO and interfacial layer thickness in the one-step and two-step deposited and annealed samples.

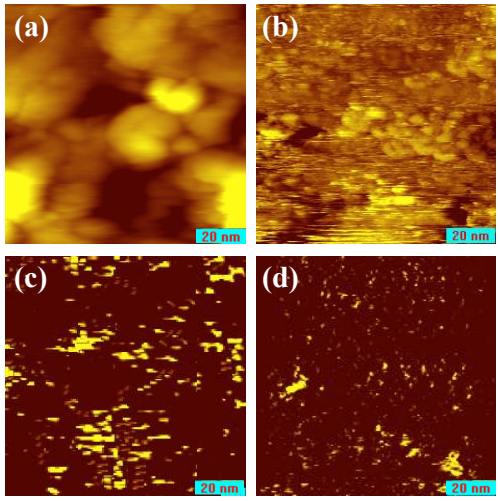


**Fig. 2** High-κ topography – (a) one-step HfSiO; bias set point, $V_s$= 3 V, $I_t$= 25 pA, and (b) two-step HfSiO; bias set point, $V_s$= 3 V, $I_t$= 24 pA. The corresponding current map (@ $V_s$ = –3.5 V) to (a) and (b) are shown in (c) and (d); bright shades correspond to locations of higher $I_t$. Area: 100 × 100 nm$^2$

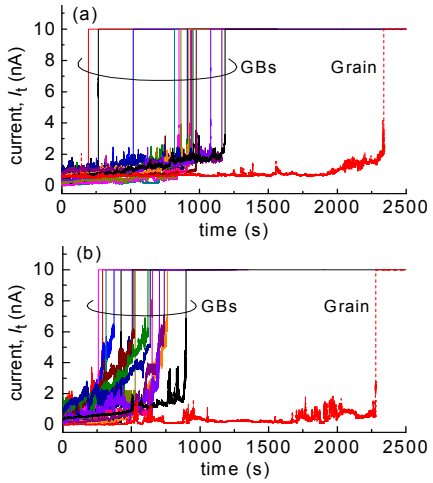


**Fig. 6** Evolution of $I_t$ during constant voltage stressing at grain boundaries (GBs) and grain in the (a) two-step, and (b) one-step HfSiO. GBs and grain are stressed at 4 V and 6 V, respectively.

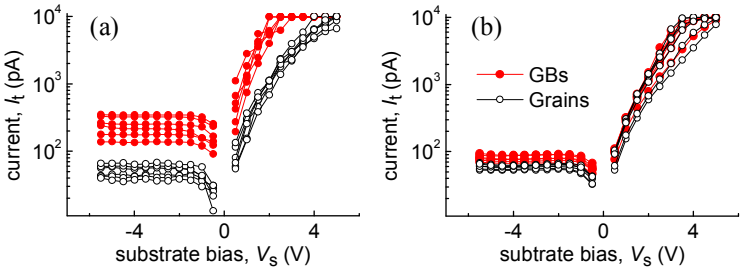


**Fig. 3** *I-V* curves at grain boundaries (GBs; filled symbol) and grains (G; open symbol) in the (a) one-step, and (b) two-step HfSiO. Bias voltage $V_s$ was swept from 5 to –5.5 V. $I_t$ is normalized to the value at 5 V.

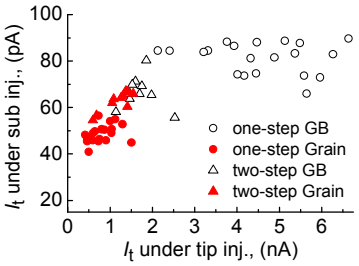


**Fig. 4** Correlation between $I_t$ under substrate injection ($V_s$ = -2 V) and tip injection ($V_s$ = 2 V) biasing for the one-step (two-step) HfSiO. Grains, filled circle (filled triangle), and grain boundaries, open circle (open triangle).

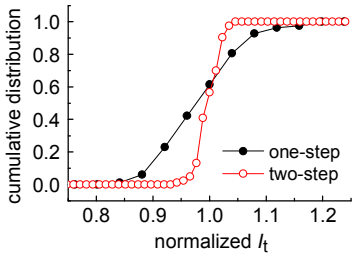


**Fig. 5** Cumulative distribution of pixels in a given scanned area having tunneling current equal or less than the normalized $I_t$ (@ 63$^{rd}$ percentile)

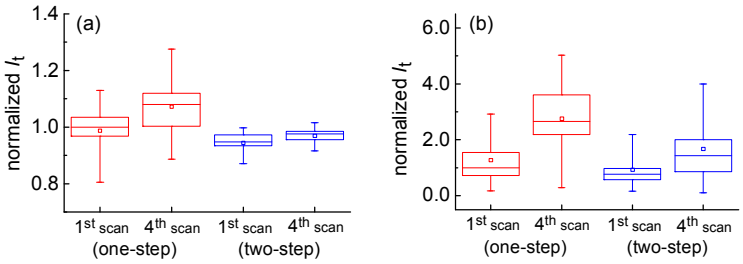


**Fig. 7** Statistical spread in current $I_t$ in a given scanned area. (a) $I_t$ measured under substrate injection biasing (probes traps in the IL[7]); (b) $I_t$ measured under tip injection biasing (probes traps in the high-κ[7]). $I_t$ is normalized to the average value of the 1$^{st}$ scan.

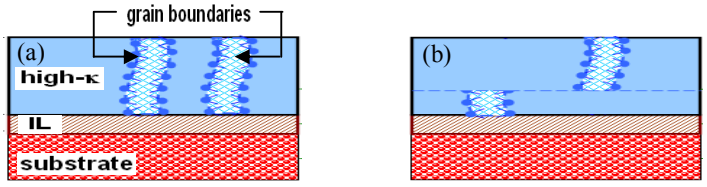


**Fig. 8** Schematic cross-sectional diagram of the (a) one-step deposited HfSiO, in which grain boundaries may propagate through the high-κ film; (b) two-step deposited HfSiO, in which grain boundaries in the two high-κ layers are, in general, misaligned.

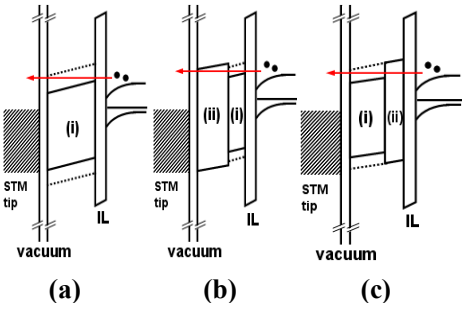


**Fig. 9** Schematic of the energy band diagrams along a certain cross-section of the one-step (a) and two-step (b) & (c) high-k stacks under the substrate injection bias. The cross-section region may include the high-κ sub-layers with (i) and without (ii) a grain boundary (percolation path).