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High-k/Metal Gate technology toward 14nm generation

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1. Introduction

Introduction of high-k/metal gate was long-awaited since it became evident that poly-Si/SiON gate structure will not provide further electrical gate thickness scaling due to inherent limit of SiON as a gate dielectrics, which originating from direct tunneling phenomena and additional electrical thickness by depletion effect of poly-Si gate electrode. This non-scalability of electrical gate thickness directly reflects to gate length scalability of CMOSFETs as expected from the scaling theory [1], that introducing innovative technology to alternate poly-Si/SiON gate stack was one of the most important issue.

After a decade of research and development, High-k/metal gate materials are currently acknowledged as alternatives of conventional poly-Si/SiON gate materials in state-of-the-art CMOS technology for 45nm logic nodes and beyond [2-5]. This was enabled after exploring numbers of high-k materials in combination of different metal materials, and eventually reaching to a consensus of Hf-based dielectrics as gate dielectrics and Ti- or Ta- based metals as gate electrodes.

This paper review current status of high-k/metal gate technology; benefits and challenges. In addition, perspective of high-k/metal gate technology toward 14 nm generations is discussed.

2. Benefits and challenges of today's high-k/metal gate technology

One of the most important benefits brought about by introduction of high-k/metal gate is reduction of electrical gate thickness with more than two orders of magnitude less gate leakage current. Electrical gate thickness at inversion condition, T_{inv}, which saturated at ~1.9 nm at 65nm node significantly reduced down to ~1.4 nm in 45nm generation with even lower gate leakage current compared to 65nm node. Short-channel effect such as DIBL, sub-threshold swing was significantly improved by scaled T_{inv}, and thus enabled to push gate length, L_g, shorter to achieve the same I_{off} compared to MOSFET with poly-Si/SiON [6, 7]. It was also demonstrated that high-k/metal gate is beneficial for current drive improvement for a given I_{off} as a result of higher inversion carrier density achieved by reduced T_{inv} and better short-channel control [6, 7].

There are still a couple of challenges remained, although industry has started implementing high-k/metal gate stacks into the platform technology.

One of the major challenges is control of effective work function, EWF, to align to Si conduction band-edge or valance band-edge due to formation of charged oxygen vacancies in high-k/metal gate system by post-processing [8]. Mid-gap like effective WF results in deeper threshold voltage, V_{th}, of MOSFETs, and thus reduced drive current than expected from the scaling theory due to less inversion layer carriers at fixed operation voltage. This is undesirable especially for high performance applications which typically require higher drive current with lower supply voltage; usually achieved by setting V_{th} low. Moreover, simulation result shows that it is necessary to achieve EWF within ~100 mV from band-edge to enjoy CMOS circuit performance benefit for high performance application [6]. Insertion of capping material into high-k/metal gate system to utilize dipoles, which form at the high-k and interfacial layer interface, is one of the promising solutions to control EWF toward band-edge [9-12]. Capping materials from group IIA and IIIB such as La, Ba and Mg are successful in this role as n-MOSFET solution [9]. Not only beneficial in terms of EWF control but also beneficial in terms of T_{inv} scaling by the increase in effective dielectric constant makes this approach very attractive. On the other hand, Al (or Al_2O_3) capping layer which is considered as p-MOSFET solution is less effective in terms of V_{th} shift and T_{inv} scaling compared to that of n-MOSFET solution according to a different arrangement of dipoles [11, 12].

Another challenge for today's high-k/metal gate technology is an unexpected growth of Si/high-k interfacial layer during post-processing caused by excess oxygen as reported in [8, 13]. It was found that much less oxygen and temperature is required to oxidize interfacial layer in some cases [8]. This unexpected interfacial layer growth would be avoidable by choosing appropriate gate metals which have high ability to getter oxygen as well as optimization of interfacial layer and process integration. It has been demonstrated that T_{inv} of 1.2 nm is achievable even with gate-first approach which serves high temperature post-processing [7].

Gate last (or replacement gate) approach would be another solution to deal with oxygen related instabilities in post-processes [3]. However, increase in process complexity and restriction in design layout would be drawbacks. Moreover, gate line is filled with high resistivity work-function metals that trade-offs between gate length scaling and increase in resistance of gate wiring would be a concern.

3. High-k/metal gate technology toward 14nm generation

Requirements for HKMG in 14nm generation are basically similar to previous generations. T_{inv} would be further scaled down to less than ~1.0 nm. One of the concerns associated with T_{inv} scaling is mobility degradation [14], but impact of mobility degradation to drive current becomes smaller as we scale L_g and MOSFET operate under quasi-ballistics transport [15]. We may able to allow ~ 50 cm^2/Vs/Angstrom degradation according to the precise analysis of MOSFET hardware combined with simulation [15]. Importance of achieving band-edge EWF as well as quality of Si to high-k interface for sub-threshold slope improvement increases as we lower operation voltage. These requirements are to enable low V_{th} to gain sufficient gate over-drive with low operation voltage.

As mentioned above, further scaling of T_{inv} less than ~1.0 nm is required for 14nm generation according to the scaling theory. Achieving the T_{inv} target would be challenging by present high-k/metal gate technology with existence of interfacial layer. Increasing effective dielectric constant by incorporating nitrogen or other elements to interfacial layer would be one solution but usually with sacrifice of reliability. Another approach is to eliminate interfacial layer itself [16-19] by either modifying deposition sequence of high-k deposition to scavenge oxygen during deposition or introduce metals in high-k/metal gate stack which scavenges oxygen afterwards. By using scavenging effect, T_{inv} of less than ~1.0 nm were successfully achieved with small influence to mobility and reliability in these reports.

In future generations, there could be a chance to use fully-depleted devices, such as FinFET [20-21], Tri-gate [22-23] or UTBB (ultra-thin box and body) [23] since these devices inherently have better electrostatics. If the device structure changes to these devices, requirements for high-k/metal gate will also change. For example, because of better short-channel control feature of fully-depleted devices, T_{inv} could be able to relax 1-2 nm compared to conventional planar device. For fully-depleted devices, V_{th} is determined not only from gate EWF but also from Si thickness (or Fin silicon width in case of FinFET and Tri-gate). For example, EWF required for these fully-depleted devices would be quarter-gap-like EWF for regular V_{th} setting MOSFETs if we take Si thickness boundary conditions into account. Realizing multi-V_{th} MOSFETs could be difficult since change in V_{th} by substrate dopant concentration is smaller compared to conventional planar-bulk. Because of this reason more than three different EWFs could be required for FinFET and Tri-gate where planar devices need two EWFs. This makes process integration of especially FinFET and Tri-gate difficult and complicated. Multi- V_{th} of UTBB could be achievable by applying back gate bias to supporting substrate [24]. However, gate etching requires high-selectivity to Si not to etch through < 10nm Si channel and source/drain.

3. Summary

High-k/metal gate technology for current node and future nodes toward 14nm generation is reviewed in this paper. For 45nm and 32nm generations, high-k/ metal gate was successfully implemented which resulted in L_g scaling and performance improvement compared to CMOS technology with poly-Si/SiON gate stacks. However, challenge of EWF control toward band-edge WF is still remained. Also, T_{inv} scaling for future node could be another concern. If device structure changes to fully-device structure requirements for T_{inv} scaling could be relaxed. Though, more challenges for process integration.

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