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Analytical Approach for Enhancement of nMOSFET Performance with Si:C Source/Drain Formed by Molecular Carbon Ion Implantation and Laser Annealing

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Introduction

Strained Si channels have widely begun to be applied to state-of-the-art CMOS devices as a booster technology of the transistor performance. The carbon doped source/drain (Si:C-S/D) is one of the most attractive booster items for nMOSFETs, and it has been extensively investigated [1-3]. Two main approaches to fabricate Si:C-S/D have been proposed. One is the recess etching at S/D before selective vapor phase epitaxy using CVD systems. The other is solid phase epitaxy (SPE) of amorphous Si:C with carbon ion implantation.

Recently, as a novel SPE technique for the Si:C-S/D formation, a combination of molecular carbon ion implantation and non-melt laser annealing was proposed [4]. Itokawa *et al*. showed that this metastable process provides the high carbon concentration of substitution ($C_{Si:C}$) and capabilities for improving nMOSFET properties.

In this paper, analytical approaches of the strained nMOSFET with Si:C-S/D are demonstrated. The channel strain induced by Si:C-S/D using molecular carbon ion implantation and leaser annealing was successfully measured by UV Raman spectroscopy for the first time. Using this particular technique, influences of the thickness of Si:C-S/D ($T_{Si:C}$) and $C_{Si:C}$ on the local stress at the channel region were investigated. The improvement of the nMOSFET performance due to the local stress induced by Si:C-S/D was also confirmed.

Experimental Procedure

Figure 1 shows the concept of nMOSFETs with Si:C-S/D formed by molecular carbon ion (C_7H_x) implantation and laser annealing. C_7H_x was implanted into the S/D region prior to the implantation of S/D impurities. Then, laser annealing was conducted for SPE and the activation of Si:C-S/D.

As basic evaluations, C_7H_x was implanted into Si substrates using the Nissin Ion Equipment Co., Ltd. Cluster Implanter: CLARIS ®. The implantation energy and the dose were varied in the range from 3 to 10 keV and from 1×10^{15} to 5×10^{15} cm^{-2}, respectively. The implantation energy and the dose of C_7H_x in this paper are expressed in terms of equivalent values of monomer carbon. $T_{Si:C}$ was measured by cross-sectional TEM. Following the Si:C-S/D formation by laser annealing at 1200 °C, $C_{Si:C}$ was measured by XRD. The stress at the channel region was measured by UV Raman spectroscopy using the particular Raman-test pattern, as shown in Fig. 2.

In electrical evaluations, characteristics of nMOSFETs with strained Si:C-S/D and relaxed Si:C-S/D were compared.

Results and Discussion

Measurement of channel strain by UV Raman spectroscopy

Figure 3 shows the thickness of amorphous Si:C layers as a function of implantation energy at doses of 1×10^{15} and 3×10^{15} cm^{-2}. The higher energy and dose provide the thick Si:C layer. The inset of the cross-sectional TEM image of the Si:C layer after the C_7H_x implantation shows the smooth Si:C/Si interface. Figure 4 shows XRD rocking curves of the Si:C layer after laser annealing. At a fixed C_7H_x implantation energy of 10 keV, $C_{Si:C}$ is higher with increasing a C_7H_x dose. On the other hand, at a fixed C_7H_x dose of 3×10^{15} cm^{-2}, $C_{Si:C}$ is maximum at a implantation energy of 8 keV, and $C_{Si:C}$ decreases at implantation energies of 10 keV or lower than 8 keV.

Figure 5 shows the cross-sectional TEM image of the Raman-test pattern. Si:C-S/D under NiPtSi is clearly observed. Since UV-ray transparently penetrates SiO_2 and its penetration depth in Si substrates is quite shallow (~5 nm), it is possible to measure the channel strain underneath the dummy SiO_2 gate by UV Raman spectroscopy.

Figures 6 and 7 show Raman peak shift at the channel region in the Raman-test pattern as a function of channel length with various C_7H_x implantation energies and doses, respectively. Negative Raman peak shift means the expansion of Si lattice due to the tensile stress induced by Si:C-S/D. Raman peak shift increases with narrowing the channel length and also with increasing the C_7H_x implantation energy and dose. The relationship between $T_{Si:C}$ and Raman peak shift is shown in Fig. 8. $C_{Si:C}$ also insets in Fig. 8. The channel strain strongly depends on $T_{Si:C}$ and $C_{Si:C}$. It is concluded that UV Raman spectroscopy is an quite effective method for measuring the channel strain induced by the Si:C layer.

Electrical properties of nMOSFET with Si:C-S/D

MOSFETs with Si:C-S/D were fabricated (see Fig. 1) and electrical properties were evaluated. Process conditions and junction properties are summarized in Table I. Two conditions of C_7H_x implantation were examined in order to investigate the simple strain effect. The simulated carbon concentration at a surface in Process-A is higher than that in Process-B. However, resultant $C_{Si:C}$ by XRD in Process-B is higher than that in Process-A. It should be noted that $C_{Si:C}$ of Process-A and -B are both lower than $C_{Si:C}$ in Fig. 4 or 8. This suggests that the combination of rapid thermal annealing (RTA) and laser annealing decreases $C_{Si:C}$. Other junction properties, such as the phosphorus profile (X_J), the junction leakage (JL) and $T_{Si:C}$, are almost identical. These results indicate that the both junction profiles are same, although the channel strain induced by Si:C-S/D of Process-B is large compared with that of Process-A.

Figure 9 shows V_t of nMOSFETs with Si:C-S/D using Process-A and -B. The V_t lowering at the short channel of Process-A and -B is almost the same, whereas V_t of Process-B is slightly higher than that of Process-A. Figure 10 shows I_{ds}-I_{off} characteristics of nMOSFETs with Si:C-S/D. 14 % gain of I_{ds} is observed in Process-B. The G_m_max ratio of Process-B to -A as a function of gate length is shown in Fig. 11. The G_m_max ratio increases with narrowing the gate length. These results are consistent with the measurement of Raman peak shift in Figs. 6 and 7. More than 25 % gain at a gate length of less than 40 nm is produced. It is concluded that the improvement of I_{ds} using Process-B is due to the local stress induced by strained Si:C-S/D.

Conclusions

The channel strain induced by Si:C-S/D formed using molecular carbon ion implantation and laser annealing was successfully measured by UV Raman spectroscopy for the first time. The thick Si:C-S/D layer and the high carbon concentration of substitution produce the large strain at the channel region. It was also confirmed that the performance of nMOSFETs is effectively improved by strained Si:C-S/D. These analytical approaches are quite valuable for promoting the development of the strained nMOSFET with Si:C-S/D.

Acknowledgements

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References

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[2] Y. Liu, et al., *VLSI Technical Digest* (2007) 44.
[3] S. S. Chung, et al., *VLSI Technical Digest* (2009) 158.
[4] H. Itokawa, et al., *Extended Abstracts of SSDM* (2009) 757.

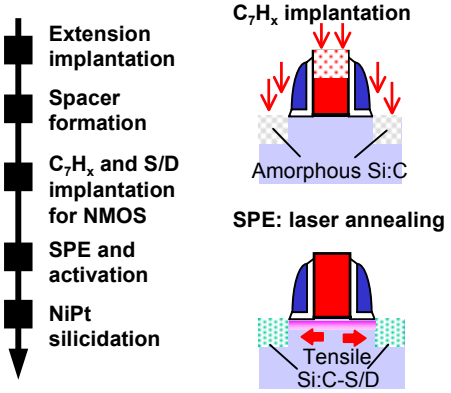


Fig. 1. Process flow of Si:C-S/D formation in nMOSFETs using C_7H_x implantation.

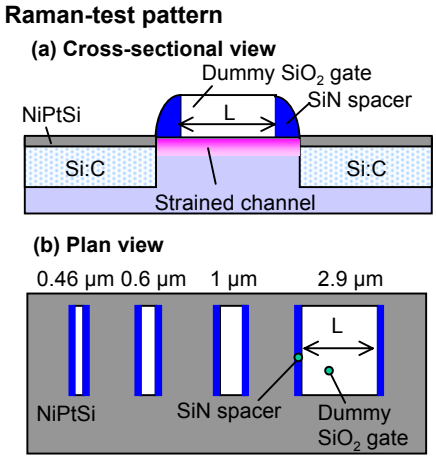


Fig. 2. (a) Cross-sectional and (b) plan views of Raman-test pattern.

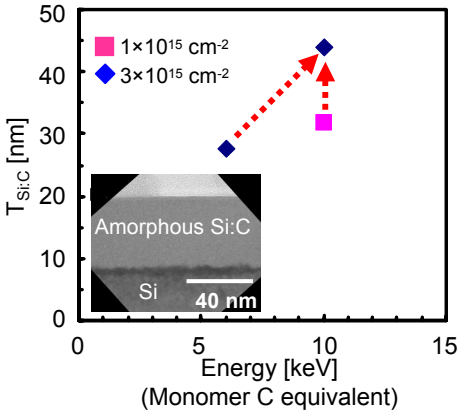


Fig. 3 Thickness of amorphous Si:C layers as a function of ion energy at doses of 3 × 10^{15} and 1 × 10^{15} cm^{-2}.

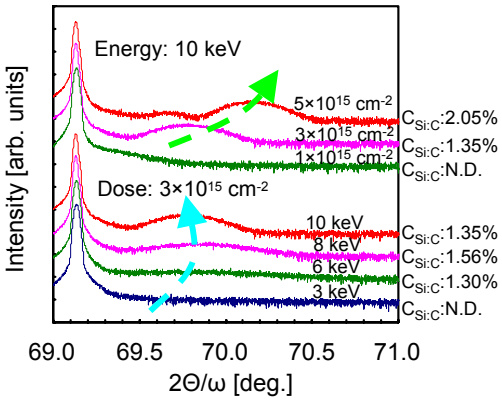


Fig. 4. XRD rocking curves of Si:C layers formed by C_7H_x implantation and 1200 °C laser annealing.

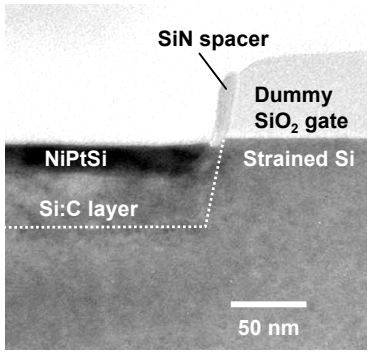


Fig. 5. Cross-sectional TEM image of Raman-test pattern.

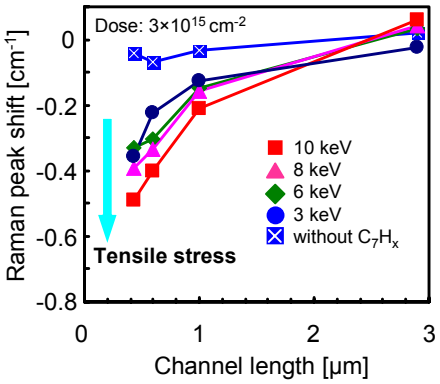


Fig. 6. Raman peak shift at channel regions as a function of channel length with various C_7H_x energies.

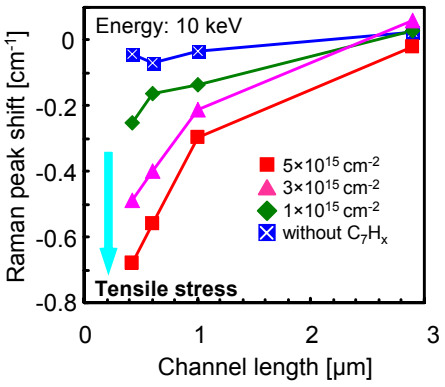


Fig. 7. Raman peak shift at channel regions as a function of channel length with various C_7H_x doses.

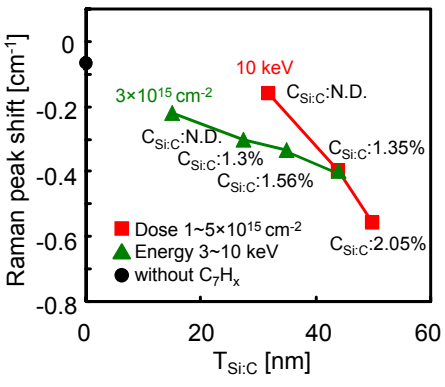
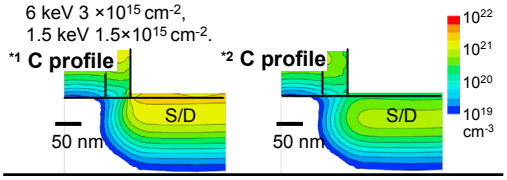


Fig. 8. Raman peak shift at a channel length of 0.6 μm as a function of thickness of amorphous Si:C layers.

Table I. Process conditions and junction properties of nMOSFETs with Si:C-S/D.

	Process-A	Process-B
C_7H_x	Multi step*1	Single step*2
P	2 keV 3×10^{15} cm^{-2}	2 keV 3×10^{15} cm^{-2}
RTA/Laser [°C]	1000/1200	1000/1200
$C_{Si:C}$ [%]	N.D.	0.33
SIMS X_J [nm]	52	52
$T_{Si:C}$ [nm]	44	44
JL nFETs [A]	0.8 × 10^{-3}	1.0 × 10^{-3}

*1 10 keV 3 ×10^{15} cm^{-2}, 6 keV 3 ×10^{15} cm^{-2}, 1.5 keV 1.5×10^{15} cm^{-2}. *2 10 keV 3×10^{15} cm^{-2}.



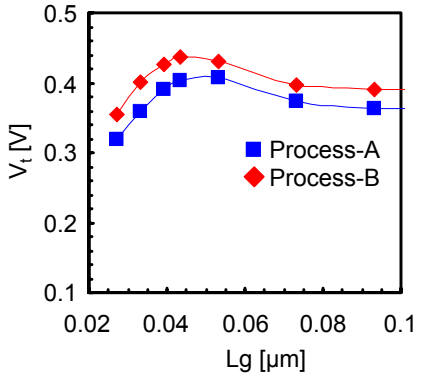


Fig. 9. V_t of nMOSFETs with Si:C-S/D using process-A and -B.

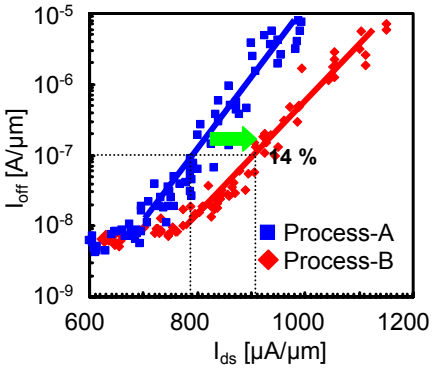


Fig. 10. I_{ds}-I_{off} characteristics of nMOSFETs with Si:C-S/D using process-A and -B.

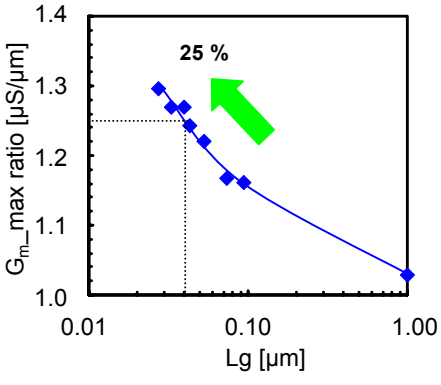


Fig. 11. G_m_max ratio of process-B to -A as a function of gate length.