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Mechanism to Achieve PMOS and NMOS Band Edge Work Function using Low Temperature Tuning Process for Low Power Application

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Abstract: Band edge work function metal gates of ~4.1eV and ~5.0eV for N- and P-MOSFETs, respectively, were achieved at low EOT (~0.9nm) and low leakage (<0.1A/cm^2 at V_g=V_{fb}-0.9V). These data result from mechanistic understanding of the low temperature process flow using WF tuning techniques with simple TiN metal and various tuning species. P-type WF was obtained by suppressing V_{fb} roll-off and N-type WF was achieved by controlling various tuning species in simple TiN.

Introduction

The need for high-k/metal gate stacks in CMOS [1,2] has led to intensive study on electrode work function tuning processes and the associated mechanisms. In the past, high temperature approaches using metal doping into high-k (La, Sc, Y for NMOS [3] and Al, Ti for PMOS [4,5]) and dual channel (Si for NMOS and SiGe for PMOS [6]) were explored. Achieving a high V_{fb} (low V_t) metal gate for future, more aggressively scaled stacks (EOT<0.9nm) continues to be a challenge due to the V_{fb} roll-off issue. Low temperature approaches have been employed to eliminate thermal budget concerns [1] and also as a mechanistic tool to understand V_{fb} roll-off associated with high temperature process [7]. This report for the first time presents a PMOS mechanism capable to suppress V_{fb} roll-off and achieve band edge PMOS work function even at EOT ~9Å at <0.1A/cm^2 at V_g=V_{fb}-0.9V through comprehensive study on V_{fb} roll-off. This study also reports a low temperature WF tuning of the same electrode for n-type WF using a doping process. A study on device failure mechanism for n-type metal gate is also discussed.

Experimental

Terraced oxide capacitors (with the SiO_2 thicknesses in the 1-4 nm range) were fabricated using Hf-based high-k (of 2 to 3 nm physical thickness) followed by the TiN films capped with doping layers. The polySi, film was then deposited and the patterned gate stack was annealed at >1000°C, then followed by the final forming gas anneal. The TiN work function tuning process is applied after S/D activation.

Results and Discussion

P-type WF. Obtaining a P-type WF value is a challenging task due to the well-known V_{fb} roll-off phenomenon, which becomes more pronounced with higher electrode WF [8]. Based on the earlier proposed understanding of the V_{fb} roll-off mechanism we implemented several options for its suppression. The proposed model explains the V_{fb} roll-off phenomenon as caused by a build-up of positive charges attributed to the oxygen vacancies at the SiO_2/Si interface, as shown in Fig. 1(a) [8]. These vacancies are formed by the metal/high-k stack induced oxygen out-diffusion from SiO_2 driven by high-temperature processes. According to the model, the V_{fb} roll-off can be reduced by using a thinner high-k film, although this is a rather limited option. Alternative approaches are to block oxygen out-diffusion from the interface by inserting an inert barrier layer between the SiO_2 and high-k (fig. 1(b)), substituting O for F in the SiO_2 (fig. 1(c)) and adding deuterium (D) in the SiO_2 (fig. 1(d)). The stronger Si-F bonds are expected to reduce the roll-off [9] and less deuterium dissociation in the D-Si bonds, would reduce O-vacancy-related defect generation at the Si interface (fig. 2). Fig. 3 demonstrates V_{fb} roll-off reduction by inserting a SiN_x layer and D incorporation. The impact of these processes is in agreement with the proposed model [8] although the V_{fb} values were slightly increased. The low temperature tuning process (fig. 1(e)) boosts WF of TiN metal gate even in the conventional gate first process but it is not expected to affect significantly the V_{fb} roll-off magnitude (fig. 4). To minimize roll-off, we start with a low WF metal exhibiting small or negligible roll-off. Then a low temperature tuning process boosts WF without inducing V_{fb} roll-off. Mechanistic understanding of V_{fb} roll-off suggests defect activation requires high temperature processing (fig. 5). This study demonstrates a breakthrough in the trade-off between the V_{fb} vs. EOT values. The obtained high 5.0 eV WF is confirmed by the direct barrier height measurements (fig. 6) [10]. Fig. 7 shows excellent C-V and gate leakage characteristics of the optimized MOSC of V_{fb} =-0.15V at EOT=0.93nm and leakage current <0.01A/cm^2 at V_g=V_{fb}-0.9V. Lower gate leakage current is attributed to higher barrier height associated with higher WF. These results are well suited for sub 28nm node low power application.

N-type WF. Fig. 8 shows tunability of the TiN work function (WF) by capping of TiN with tuning species (TS). TiN WF is in a range of 4.1~4.6 eV depending on TiN thickness and following annealing temperature. Low WF is most likely due to TS element accumulation at the HK/TiN interface (fig. 9). The TiN WF change due to TS doping is also confirmed by the direct measurements of the barrier height change using the J-V technique [10] as seen in Fig. 10. Low temperature tuning process requires different dopants rather than lanthanide metal elements (La, Gd, Sc) that were usually utilized in high temperature tuning approaches because of the very different process window. However, TS doping may also cause device failure when the annealing is performed at the above critical temperature. The J-V characteristics of the terraced oxide MOSCs with the TiN/TS gate stack annealed at 480°C show initial failure regardless of the bottom SiO_2 thickness, Fig. 11 (inset TEM images in fig. 11). Backside SIMS data show that annealing at 480°C results in a significant TS diffusion through the TiN, HK and even thick SiO_2 films (fig. 12). TS clusters are also observed in the active area after Si is removed for the backside SIMS measurements (fig. 13). Further analyses suggest the TS-induced device failure could be due to a conductive filaments formation in the gate stack by the localized TS diffusion at a critical temperature. Fig. 14 shows excellent C-V and gate leakage characteristics of the optimized NMOSC showing -0.9V V_{fb} at 0.93nm EOT and <0.1A/cm^2 at V_g=V_{fb}-0.9V.

Conclusion

To obtain high WF, we employed a low work function metal, which is characterized by minimal V_{fb} roll-off, combined with low temperature tuning process to increase the effective WF value while maintaining minimal V_{fb} roll-off. This approach has resulted in a targeted WF value of 5.0 eV without EOT penalty. Low WF was achieved by using TiN/TS and a low temperature process to control TS doping. Annealing above a certain critical temperature is shown to result in device failure due to a metal-induced conductive filament formation. This CMOS-compatible tuning process can also be applied to both dielectric-last/metal-

last and dielectric-first/metal-last integration schemes.

Reference; [1] K. Mistry, et. al., IEDM 2007. [2] S. Natarajan, et al., IEDM 2008. [3] P. Sivasubramani, et. al., VLSI 2007. [4] H. Alshareef, et. al., *Appl. Phys. Lett.*, vol. 88, 2006. [5] H. Takahashi, et. al., IEDM 2009. [6] R. Harris, et. al., VLSI 2007. [7] L.-Å. Ragnarsson, et. al., IEDM 2009. [8] G. Bersuker, et. al., ESSDERC 2008. [9] K. Choi, et. al., IRPS 2007. [10] H. C. Wen, et. al,, *Elect. Dev. Lett.*, vol. 27, 2006.

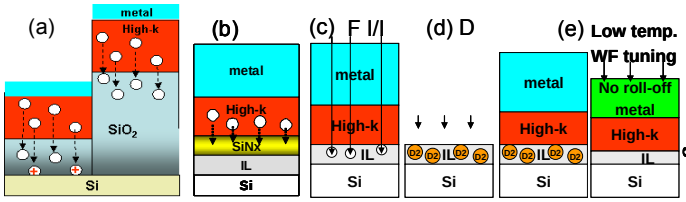

Fig. 1 (a) Schematic V_{fb} roll-off model based on oxygen deficiency in IL. Based on the model, several approaches are suggested to oxygen vacancy (b) SiN_x layer between high-k and IL for blocking oxygen or oxygen vacancy transport, (c) F ion implantation for oxygen vacancy passivation, (d) pre-incorporation of D into IL, and (e) low temperature WF tuning of no or negligible V_{fb} roll-off metal gate.

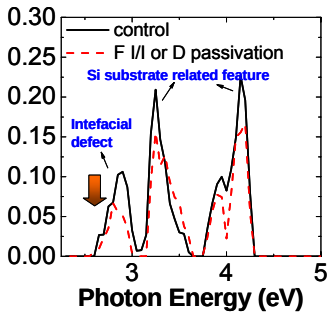

Fig. 2 Spectroscopy Elliposmetry measurement data suggests reduced interfacial defect by F I/I and annealing in a deuterium (D) ambient.

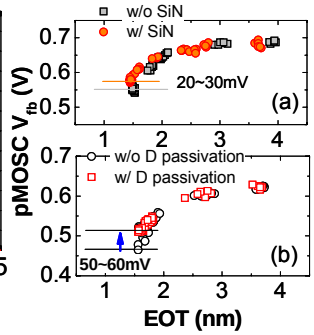

Fig. 3 V_{fb} roll-off suppression by (a) adding SiNx into HK/metal gate and (b) pre-incorporation of deuterium (D) into IL.

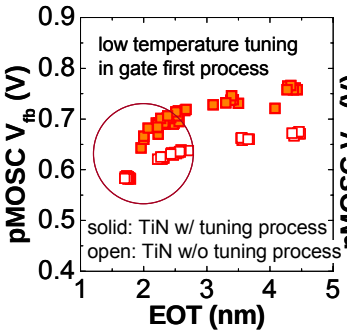

Fig. 4 Low temperature tuning process in both gate first and gate last process boost WF but it contributes to EOT increase and does not help suppress V_{fb} roll-off.

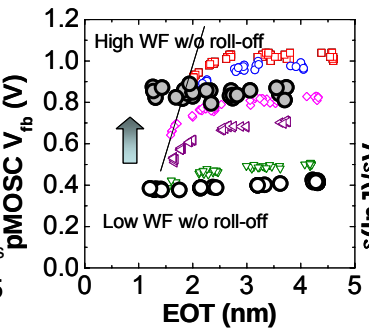

Fig. 5 Low WF metal with tuning process in low temperature process shows WF boost while maintaining no V_{fb} roll-off.

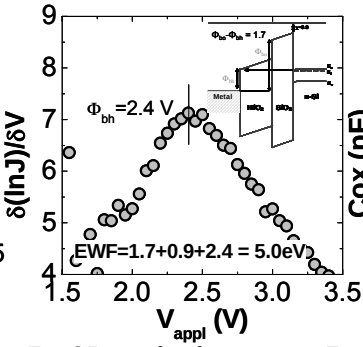

Fig. 6 Barrier height measurement confirms achieving 5.0eV WF by low temperature tuning process.

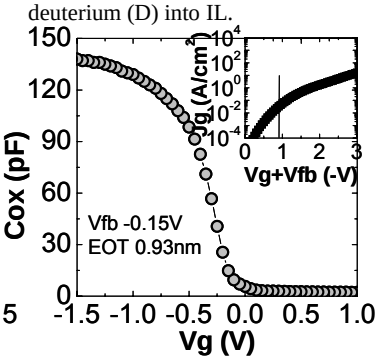

Fig. 7 C-V and J-V characteristics of NMOSC with HK/TiN/TM that got optimized low temperature process for P-type WF tuning without EOT penalty.

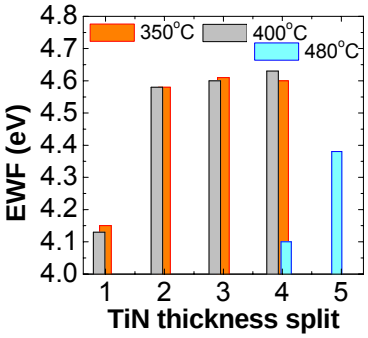

Fig. 8 Effective work function (EWF) of TiN with tuning species (TS) depending on TiN thickness and annealing temperature.

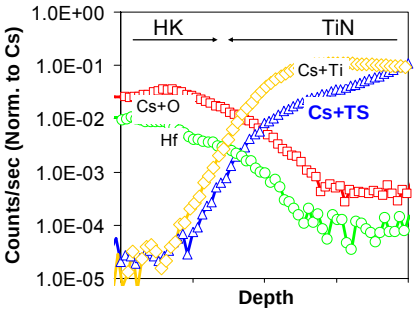

Fig. 9 Backside SIMS of gate stack with low WF TiN metal gate (split #01 in Fig. 1). Analyses were made after backside Si is completely removed. TS is diffused through TiN and accumulated at HK/TiN interface causing WF shift to 4.1eV.

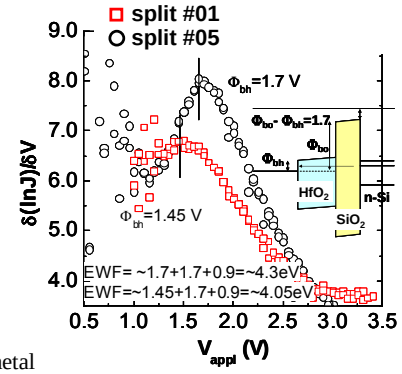

Fig. 10 Barrier height measurement confirms WF change of TiN (split #01 and #05 in Fig. 8).

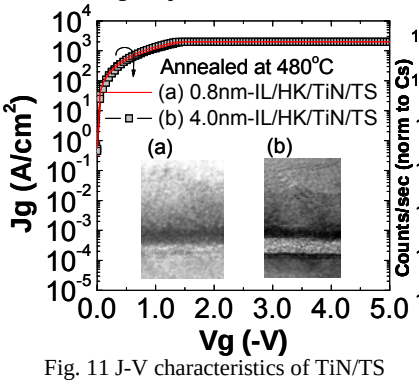

Fig. 11 J-V characteristics of TiN/TS MOSCs with (a) thin and (b) thick bottom SiO_2 that got annealing at 480°C.

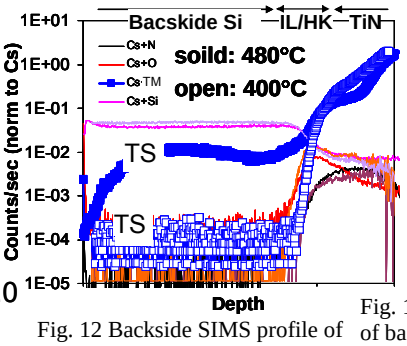

Fig. 12 Backside SIMS profile of 4.0nm-IL/HK/TiN/TS MOSCs that got annealing at 400°C and 480°C.

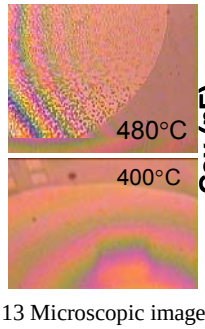

Fig. 13 Microscopic images of backside area that got SIMS sputtering. Defects are observed on the sample got annealing at 480°C.

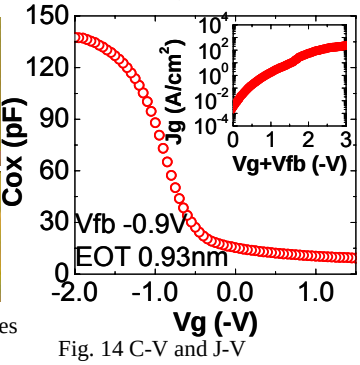

Fig. 14 C-V and J-V characteristics of NMOSC with HK/TiN/TS that got process optimization.