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Asymmetric Gate-oxide Thickness Four-terminal FinFETs Fabricated using Low-Temperature and Atomically Flat interface Neutral-Beam Oxidation Process

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1. Introduction

The scaling down of MOSFETs requires gates to be less than 23 nm long[1]. In this generation of devices, it is difficult to improve performance of MOSFET devices by only down-scaling because of short channel effect. To solve these problems, new MOSFET structures, such as FinFET, have been widely investigated. There are two types of FinFETs: the three-terminal (3T) FinFET and the four-terminal (4T) FinFET.[2-5] Both have an ultrathin silicon (Si) fin structure pinched by dual gate electrodes for controlling short channel effect while maintaining a high drive current. Additionally, because the 4T-FinFET has independent dual gate electrodes, its threshold voltage (V_{th}) can be controlled independently. However, 4T-FinFETs had symmetrically thin gate oxides on both channels, resulting in large subthreshold slope (S-slope) due to the negative effect of the high second gate controllability.[6] To attain a good S-slope, the asymmetric gate oxide thickness (T_{ox}) has been suggested.[4] Figure 1 shows the concept of asymmetric T_{ox} 4T-FinFET. For the asymmetric T_{ox} 4T-FinFETs, not only flexible V_{th} controllability, but also low S-slope can be realized due to low effective body capacitance C_{Beff} ($=C_{ox2}C_{Si}/(C_{ox2}+C_{Si})$). However, it is difficult to fabricate gate dielectric film with different thicknesses on each side by the conventional thermal oxidation (TO) process owing to isotropic oxidation and lattice plane dependence of the oxidation rate. Even though some approaches have been developed, the fabrication process is very complex.[4,5] Additionally, high temperature TO process induces residual stress at Si/SiO_2 interface, which increases interfacial state density (D_{it}), resulting in a high leakage current.[7]

To tackle these problems, we proposed the neutral beam oxidation (NBO) process as an alternative to the thermal oxidation (TO) process.[8] NBO can realize anisotropic oxidation and lattice-plane-free process due to collimated oxygen neutral beam bombarding with Si surface and then simply generate high quality SiO_2. Also, the electric characteristic of SiO_2 films fabricated by NBO at low temperature (< 300 °C) is almost the same as that of films fabricated by TO.[9] In this study, we fabricated 3T-FinFET and symmetric/asymmetric T_{ox} 4T-FinFETs and evaluated their performances by using the simple NBO process.

2. Experiments

Figure 2 shows the schematic process flow of 3T- and 4T-FinFETs. A silicon-on-insulator (SOI) wafer was used to investigate the FinFETs with n-channel. The pattern for fin structure was determined by electron beam (EB) lithography, and then the fin structure was fabricated by NB etching. After that, a gate dielectric film was grown on each sidewall of the fin structure in two gate areas: driving gate (G1) and control gate (G2). NBO films were grown on each sidewall of the fin structure with two steps by tilting the sample at +30 and -30° sequentially as gate dielectric films, as shown in Fig. 3. Gate dielectric film was covered with n+ polycrystalline-Si (Poly-Si). After a gate electrode was formed using inductive coupled plasma (ICP) etching, ion-implantation (P) into the extension of the source/drain (S/D) was performed. Then, in the case of 4T-FinFET, the poly-Si gate was separated by using a developed resist etch-back process[10], as shown in Fig. 4. After the poly-Si gate was revealed by thinning the EB resist, the poly-Si gate separated using ICP-reactive ion etching (RIE) and the poly-Si gate over the Si-fin connected to the each side of the gate was completely removed. Finally, S/D was activated at 900ºC for 2 seconds, and the devices were sintered at 450ºC in 3% H_2 ambient after the aluminum electrode metallization.

3. Results and discussions

We measured the drain-current versus gate-voltage (I_d-V_g) characteristics of 3T-FinFETs, as shown in Fig. 5. The S-slope of the FinFET fabricated by NBO was apparently improved more than that of the one with conventional TO. We speculated that this improved S-slope is due to the fact that the SiO_2 film fabricated by NBO had a lower D_{it} than that fabricated by TO. We also calculated effective mobility (μ_{eff}) of the 3T-FinFETs, as shown in Fig. 6. This result shows that the μ_{eff} of the 3T-FinFETs fabricated by NBO was improved in high carrier density area. This improved μ_{eff} is considered to be a result of the atomic-level flatness at the SiO_2/Si interface. For a three-dimensional structure, in the case of TO, D_{it} and roughness increase at the edge of the fin owing to the dependence of what is on the lattice plane. In contrast, in the case of NBO, the low D_{it} and low roughness are due to the fact that NBO is a low-temperature and lattice-plane-free process.

Figure 7 shows the cross-sectional transmission electron microscope (TEM) image of the asymmetric (T_{ox1}=2.5nm, T_{ox2} = 4nm) T_{ox} 4T-FinFET. The poly-Si gate was successfully separated by gate separation etching. Figure 8(a) and

(b) show the I_d-V_{g1} characteristics of symmetric (T_{ox1} = T_{ox2} = 2.5nm) and asymmetric (T_{ox1}=2.5nm, T_{ox2} = 4nm) T_{ox} 4T-FinFETs, respectively, and the V_{th} (V_{g1} at I_d = T_{fin} / L_g × 10^{-7} A/μm) and S-slope as a function of V_{g2} for both 4T-FinFETs are plotted in Fig. 8(c). The symmetric T_{ox} 4T-FinFETs clearly exhibit flexible V_{th} controllability by applying a bias voltage to G2, as shown in Figure 8(c). Specifically, note that V_{th} shift rate (defined by $-\delta V_{th}/\delta V_{g2}$) is very large in the depletion condition ($V_{g2} < V_{th(3T)}$ = -0.4V ($V_{th(3T)}$ is V_{th} in the 3T-mode)). On the basis of this result, to prevent S-slope degradation, we investigated the asymmetric T_{ox} 4T-FinFETs. We found that V_{th} shift rate becomes lower and S-slope is improved as T_{ox2} increases. Here, we calculated $|\delta(\text{S-slope})|/|\delta V_{th}|$ (S/V_{th}) to investigate the performance of symmetric/asymmetric T_{ox} 4T-FinFET. The smaller the S/V_{th} value, the better the performance of 4T-FinFET. The S/V_{th} values of the asymmetric and symmetric T_{ox} 4T-FinFETs are 71 and 322, respectively, in the depletion condition. This result indicated that the performance in the symmetric T_{ox} 4T-FinFET is effectively improved by introducing asymmetric T_{ox} for the independent gates.

4. Conclusions

The S-slope and μ_{eff} of the fabricated 3T-FinFET with NBO were slightly improved owing to the low D_{it} and atomic-level flatness, respectively. Flexibly V_{th}-controllable symmetric and asymmetric T_{ox} 4T-FinFETs with the NBO process have been successfully fabricated by simpler fabrication processes. The performance of the asymmetric T_{ox} 4T-FinFETs was drastically improved more than that of the symmetric T_{ox} 4T-FinFETs owing to the slightly thick V_{th} control-gate oxide. These results demonstrate the great potential of the NBO process for fabricating three-dimensional 4T-FinFETs.

References

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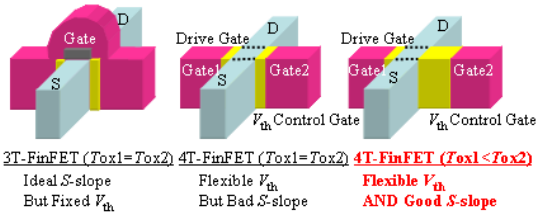

Fig.1 Concept of asymmetric T_{ox} (thin drive-gate oxide and thick V_{th}-control-gate oxide) 4T-FinFET. For the asymmetric T_{ox} 4T-FinFETs, not only flexible V_{th} controllability, but also low S-slope can be realized due to low effective body capacitance C_{Beff} (=$C_{ox2}C_{Si}$/ (C_{ox2}+C_{Si})).

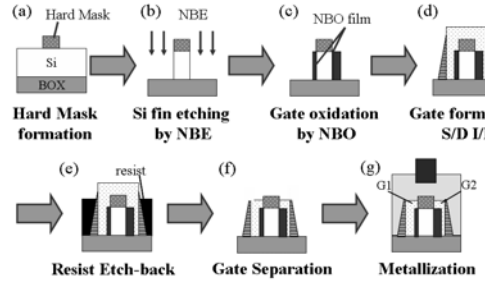

Fig. 2 Fabrication process flow of 3T- and 4T-FinFET. Fin is fabricated by NBE. Gate oxide film is formed by NBO.

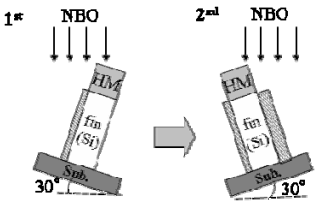

Fig. 3 Scheme of NBO process for fabricating gate oxide film

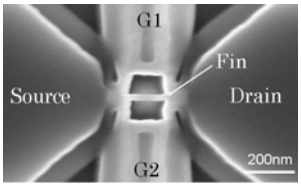

Fig. 4 SEM image of FinFET after the gate separation etching

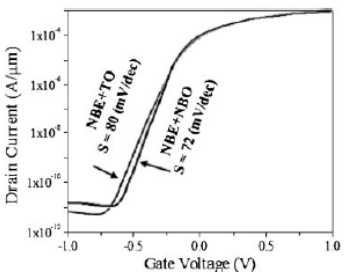

Fig. 5 Id-Vg characteristics of 3T-FinFET.

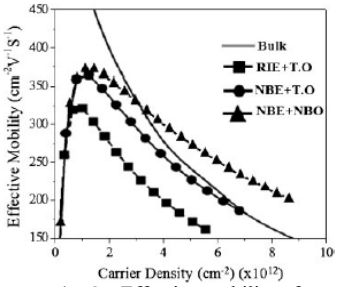

Fig. 6 Effective mobility of 3T-FinFET.

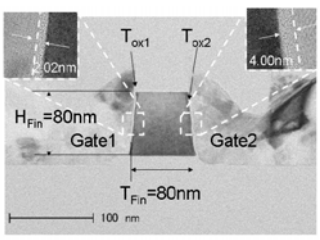

Fig. 7 Cross-sectional TEM image of fabricated asymmetric Tox 4T-FinFET

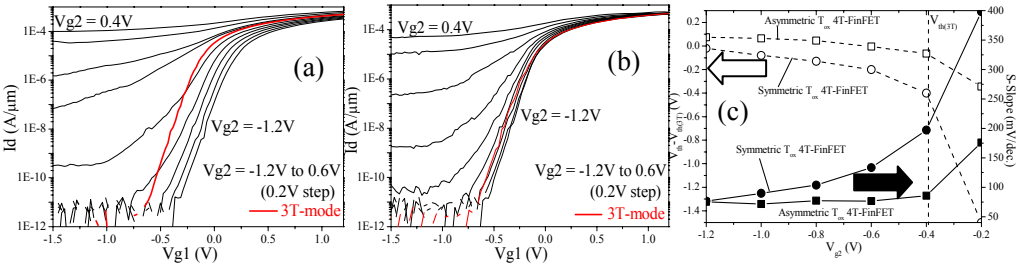

Fig. 8 Id-Vg1 characteristics in 4T-FinFETs for (a) symmetric T_{ox} (T_{ox1}=T_{ox2}=2.5nm), (b) Asymmetric T_{ox} (T_{ox1}=2.5nm, T_{ox2}=4nm). (c) Vth versus S-slope as a function of V_{g2}.