Extended Abstracts of the 2010 International Conference on Solid State Devices and Materials, Tokyo, 2010, pp982-983

Overview and Challenges in Source/Drain Formation Technology in High Performance Transistors

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Abstract

Source and drain formation technologies which are required in next generation Si devices such as memory LSIs and system LSIs are overviewed and the new challenge for the future devices are discussed in this paper.

1. Introduction

In high performance transistors which are used in Si LSIs, the miniaturization of channel length continued to around 30nm so far in order to shorten the traveling time of charge carriers from source to drain region. The miniaturization of channel length requires the shallowing of the depth in sources and drains. For mitigating short channel effects, the extensions as shallow as 20nm or less are necessary for sources and drains.

On the other hand, low resistivity metal silicide films on source and drain diffusion layers are indispensable for lowering parasitic resistances of sources and drains, i.e., SALICIDE is formed on source and drain. The metal silicide films form by consuming some thickness of Si. Recently NiSi films are usually used in SALICIDE and a 10nm Ni film consumes.18-19nm of Si to form 22nm of NiSi. If the distance between NiSi and pn junction decreases to 50-60nm, pn junction leakage current abruptly increases to unacceptable level. Therefore, the pn junction depth of the contact region should be much deeper than the extension regions.

Figure 1 schematically shows the roles of impurity doped region for better performance of MOSFETs.

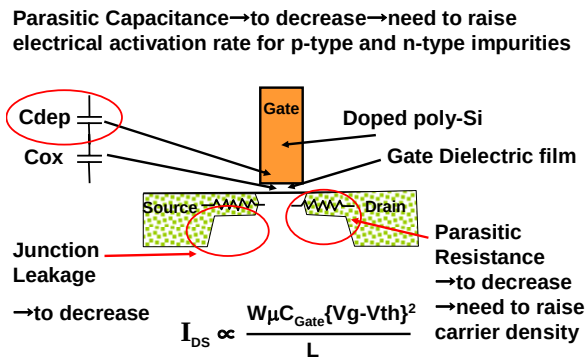

Fig. 1 Roles of impurity doped region for better MOSFET performance.

As shown in Fig. 1, the main roles of source and drain are to lowering parasitic resistance and pn junction leakage current even if gate length becomes a few tens nm. In this figure SALICIDE is omitted for simplifying the roles of diffusion layers in source and drain. SALICIDE on source and drain strongly affects pn junction leakage current and the contact resistance between the silicide and a doped Si layer.

In extension region there are several requirements for better performance of MOSFETs. First the electrical activation rate should be higher especially for ultra-shallow junction. Secondly the crystal damage caused by ion implantation should be annealed. Thirdly the abruptness of profile near the pn junction should be steeper as high as possible.

2. Enhancement of electrical activation for impurities

In order to highly activate impurities in Si, it is necessary to increase solubility of impurity in Si. Solubility of impurity in semiconductors was discussed by Trumbore 50 years ago. [1] And the solubility data were rechecked by Borisenko and Yudin.[2] Table 1 shows the solubility values of B, As and P in Si at 1000°C and 1200 °C referred to Ref. 3.

	1000℃	1200℃
B	$2x10^{20}cm^{-3}$	$6x10^{20}cm^{-3}$
As	$3.5x10^{20}cm^{-3}$	$1.5x10^{21}cm^{-3}$
P	$3.8x10^{20}cm^{-3}$	$5x10^{20}cm^{-3}$

Table 1 Solubility of B, As and P in Si [3]

Generally the solubility of impurities increases with temperatures and the higher temperature, the higher activation rate. Since the diffusion length of impurities increases with temperatures, annealing length should be shorter for reducing the diffusion length. If the pn junction depth of the source/drain extension needs to be less than 20nm, ion implantation and plasma doping are able to form the depth profile ranged from 5 to 10nm, therefore, the diffusion length of impurities needs to be less than 10-15nm. Considering the diffusion constant of B which has the largest diffusion constant among impurities described above. The allowable time length for 1000 °C, 1100 °C, 1200 °C and 1300 °C is estimated to be less than 1sec, 0.2sec, 0.02sec

and 0.002sec (2msec), respectively.

For millisecond annealing, flash lamp annealing (FLA) is very effective to control the pulse length of heating and usually combined with lower temperature halogen lamp annealing, i. e., spike RTA. [4-16] The thermal budget for annealing defects and controlling diffusion length is necessary to considered each activation energy. [17-18]

3. Control of abruptness for impurity profiles

It is possible to obtain shallower Xj with lower sheet resistance by using millisecond annealing as shown in Fig. 2. FLA and laser annealing are able to form shallower Xj with lower sheet resistance as compared with spike RTA,. [14]

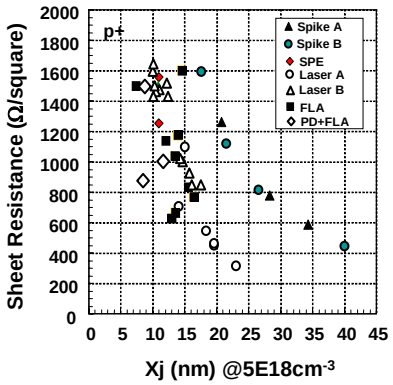

Fig. 2 Sheet resistance as a function of Xj for boron.

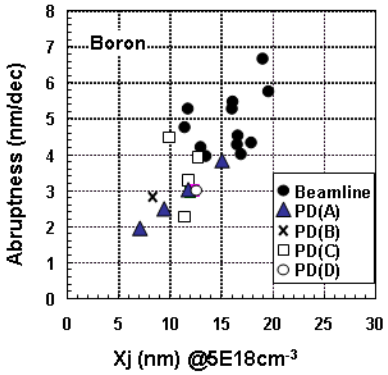

Fig. 3 Abrupness as a function of Xj for boron.

In order to control the abruptness of pn junction, it is necessary to control not only as implanted profile tail region but the enhanced diffusion length of impurities. Plasma doping has an advantage of steeper profile after millisecond annealing and halogen lamp annealing. Fig. 3 shows the abruptness as a function of Xj after millisecond annealing. It is clear that the abruptness of less than 3nm/dec can be successfully obtained by using plasma doping technology. The performance of pMOSFET with 20nm or less of Lg was improved due to the improvement of abruptness of B profile. [19]

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