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Raised S/D for Advanced Planar MOSFET devices: Challenges and Applications for the 20nm Node and Beyond

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1. Introduction

Raised S/D (RSD) epitaxy provides a significant knob to meet the short-channel and leakage requirements of highly scaled MOS devices [1]. In more recent planar technologies using thin-body devices, faceted RSD epitaxy was presented as a key process that enables performance, overcoming major device issues such as doping control and parasitic capacitance [2][3]. However, as device physical dimensions continue to scale, faceted RSD epitaxy integration presents new challenges in term of loading effects, facet reproducibility and control. In this paper, the feasibility and integration of flat and faceted RSD silicon epitaxy are investigated. As a function of process conditions, different facet features can be generated. The ability of cyclic deposition to achieve either flat or faceted RSD epitaxy at low temperature with a very good repeatability will be discussed. Finally, the pitch dependence of the faceted cyclic epitaxy will be highlighted and the extendibility of this technique to the 20nm node and further will be addressed.

2. Experiments

All RSD epitaxy experiments were carried out using an industrially available Applied Materials 300mm-wafer RT-CVD reactor starting from patterned SOI wafers featuring thin 8nm silicon channel and 6nm SiN spacers (figure 1). These test wafers were patterned using the 20nm design ground rules with different gate pitches and as well as large 100µmx100µm isolated areas on the same wafer. Regarding the process conditions, a low total pressure of 20Torr was used in all these experiments to ensure minimized loading effects with a standard chlorinated DCS/HCl gas mixture and H_2 as carrier gas. The RSD morphology obtained after both standard and cyclic epitaxy next to SiN spacers will be compared for different process conditions. Controlling the HCl concentration or exposure time at a given concentration enables us to generate two distinct RSD profiles: a conventional flat shape showing epitaxial growth along [100] direction or a faceted RSD epitaxy featuring both (111) and (311) facets next to SiN spacers.

3. Results and Discussions

RSD using standard DCS/HCl/H_2 gas mixture:

First, we will consider the different RSD epitaxy shapes that can be generated with a standard chlorinated chemistry using direct injection of DCS/HCl. The temperature range of 750°C - 800°C was studied at constant DCS mass flow but various HCl concentrations. The impact of the HCl partial pressure is presented in figures 2a and 2b. As the DCS/HCl ratio is decreased from 1.2 to 1 at 800°C, epitaxy shape is modified from flat to faceted. Indeed, HCl gas is the main parameter which controls the facet extension and faceted epitaxy can be obtained in a wide range of temperatures, as highlighted in figures 2b and 2c. With a standard epitaxy, only the (311) facet was observed next to SiN spacers and at a fixed growth rate, the extension of this particular plane becomes less pronounced when the temperature is lowered as the ratio $r_{311}=GR_{(311)}/GR_{(100)}$ increases [4]. Therefore, only a flat epitaxy delimited by the (100) plane is observed at very low temperature (750°C, figure 2d).

RSD using cyclic epitaxy/etch with DCS/HCl/H_2:

Cyclic epitaxy and etch technique can be attractive as it gives access to lower deposition temperatures with an acceptable growth rate as no HCl is added during the deposition steps [5]. In this case, we studied the temperature range of 700°C-750°C with constant DCS, HCl mass flow and deposition time. The process time of the etch cycles t_{etch} was tuned at each temperature to generate either a flat or faceted epitaxy. As we can see on figure 3, at 750°C and 725°C a (111) faceted epitaxy can be obtained at t_{dep}/t_{etch}=1.1 and 0.71, respectively while at 700°C no facet can be observed in a wide range of t_{dep}/t_{etch} ratios down to 0.66. However, stable (111) facets are obtained at 750°C using cyclic epitaxy which proves the capability of this process to generate flat or faceted RSD epitaxy.

Flat and Faceted RSD comparison: pitch dependence

Finally, we compare the gate pitch dependence of both flat (figure 4a) and faceted epitaxy (figure 4b). For flat cyclic epitaxy, the thickness variation is small, standard loading effects are observed from large 100µmx100µm pads down to 80nm pitch (30nm space). That shows a great extendibility of this process for spaces as tight as 30nm and below. On the other hand, faceted epitaxy exhibits a mix of both loading and geometrical effects due to the spatial proximity of the facets. As highlighted in figure 5, we observe a linear regime and then saturation in thickness when the facets are merging together. In this configuration, the growth is self-limited as there is no more nucleation along both the SiN spacers and [100] direction. This pitch limitation is only observable when the space is comparable to the targeted RSD thickness and for given (hkl) planes, the saturation thickness can be extracted by simple geometrical considerations. We report in figure 6a the maximum RSD thickness we can grow as a function of the technology node for simple epitaxy facet features. With this work, we demonstrate that sharp (111)-facetted RSD using cyclic epitaxy is extendable beyond 20nm node. However, it should be emphasized that obtaining a pure (111) profile is challenging as secondary high-order (hkl) planes usually appear at the (111) plane junctions, inducing a self-limitation of the growth before the geometrically expected saturation thickness (figure 6b).

3. Conclusions

We have shown the excellent capabilities of the cyclic deposition/etch process to achieve both flat and faceted epitaxy at low temperature. For a flat epitaxy no pitch dependence was observed unlike faceted epitaxy. We demonstrated that for given (hkl) facets next to the SiN spacers there is saturation in thickness which is related to the device layout. Finally, low temperature cyclic RSD epitaxy can be achieved with good control and repeatability of the process and will be therefore a key element to overcome the issues associated with the most aggressive technology nodes.

Acknowledgements

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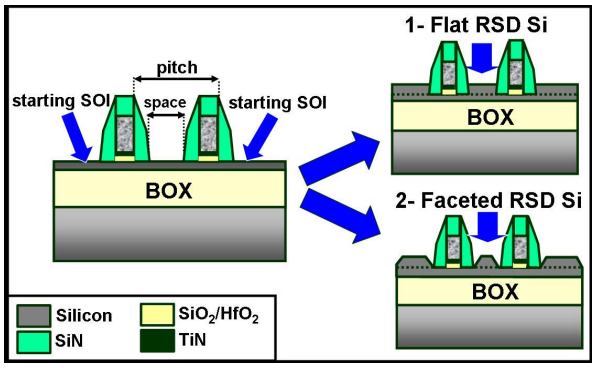

Figure 1: Experimental – starting from patterned SOI wafers we can generate both flat and faceted RSD epitaxy next to SiN spacers

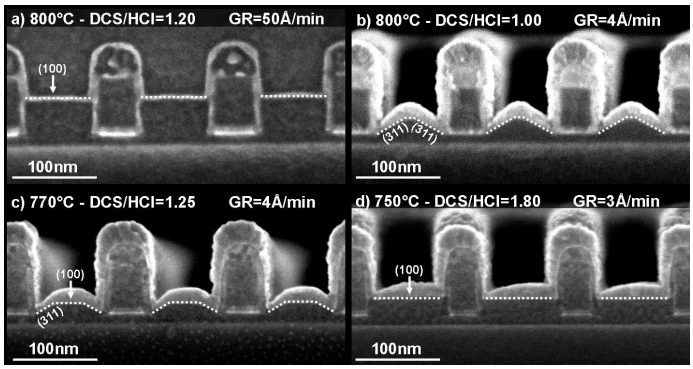

Figure 2: a) and b) are showing the effect of HCl concentration on facet appearance. The generated (311) facet is less pronounced as temperature drops as highlighted in c) and d).

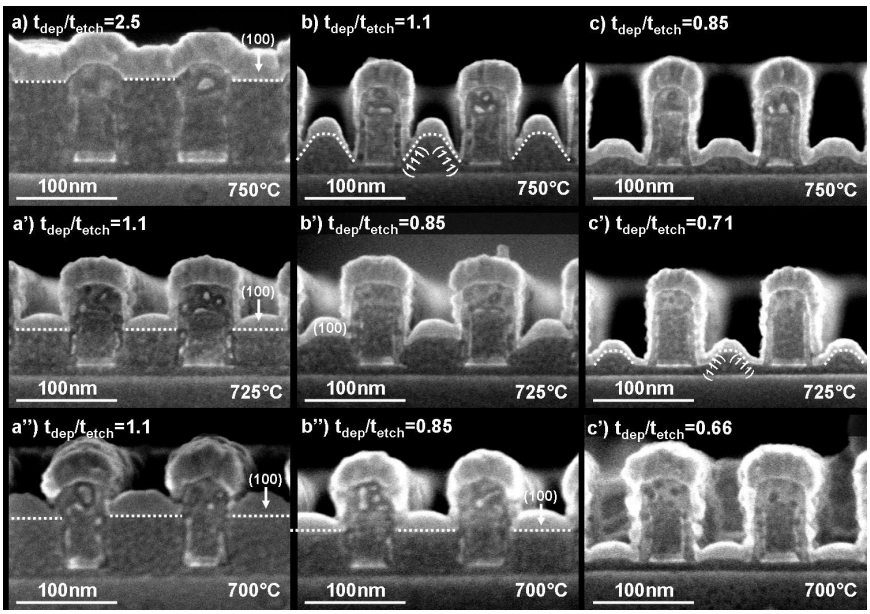

Figure 3: SEM cross-section after RSD using cyclic deposition/etch at various temperatures: 750°C (top), 725°C (middle), and 700°C (bottom) and for different t_{dep}/t_{etch} conditions.

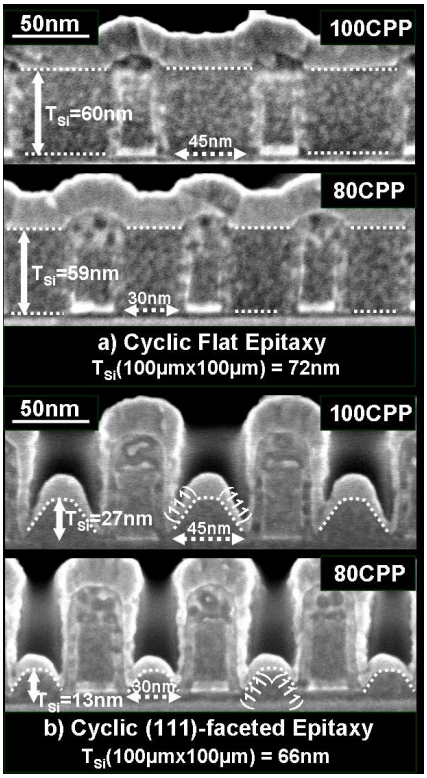

Figure 4: TEM cross-section showing the gate pitch dependence of RSD epitaxy using cyclic deposition/etch at 750C in the case of (a) a flat epitaxy next to SiN spacers and (b) a faceted (111) RSD epitaxy. Are also reported the ellipsometry measurement on large 100µmx100µm zones evidencing the space dependence of the faceted RSD process.

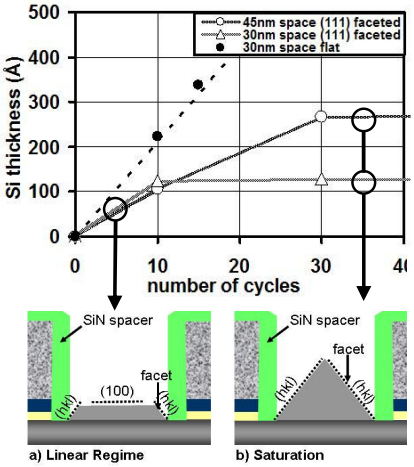

Figure 5: RSD thickness obtained for flat and (111)-faceted shapes as a function of the number of cycles. 30nm and 45nm spaces are showing a common linear growth regime (a) followed by a saturation mode when facets are merged (b)

Node	28nm	20nm	15nm
Device Pitch (nm)	120	80	60
space (nm)	60	30	20
Year	2010	2012	2015
	Maximum thickness (nm)		
Faceted (111)	~40	~20 (*13)	~14
Faceted (311)	~20	~10	~7
Flat (100)	∞	∞	∞

a) * this work

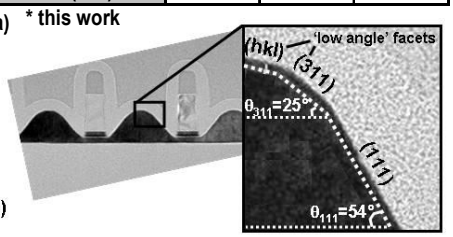

Figure 6: a) Table showing the extendibility of cyclic RSD process towards the various technology nodes. In the case of the flat epitaxy no pitch effect is observed unlike faceted RSD. b) TEM cross section evidencing the multi-faceting at the (111) facet boundaries.

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