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Raman Spectroscopy Measurement of Silicidation Induced Stress in Si and its Impact on Performances of Metal Source/Drain MOSFETs

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1. Introduction

Silicide is the key material for fabrication of metal source and drain (S/D) structures in advanced CMOS devices because of low formation temperature, low resistivity, and applicability of self-aligned process. While silicide-based metal S/D is expected to solve parasitic resistance issues in future devices such as ultra thin SOI, FinFET and SNW FETs, we draw attentions to the mechanical properties of silicides. Typical properties of silicides and silicon are listed in **Table 1**. A noticeable difference is the coefficient of thermal expansion (CTE) [1-3]. It brings a matter when the metal S/D is prepared by silicidation reaction (**Fig. 1**). As the wafer is cooled down from the silicidation temperature to room temperature, stress is induced into Si region because of the volume difference of materials at room temperature (**Fig. 2**).

In this work, we focus on silicidation induced stress in silicon. Degrees of stresses are compared in two silicide phases. The impact of silicidation induced stress on electrical performances was examined by metal S/D MOSFETs.

2. Experimental

NiSi and $NiSi_2$ films were prepared by sputter deposition of Ni films on hydrogen-terminated Si surface and annealing at 500ºC. Although 500ºC is the typical silicidation temperature for NiSi phase formation, our developed SiN buffer layer technique accomplishes formation of high temperature $NiSi_2$ phase at 500ºC without intervention of any low temperature phases [4-6]. Epitaxial growth of $NiSi_2$ film with uniform thickness is confirmed in previous studies. NiSi film, on the other hand, is poly-crystalline with random orientation. Thicknesses of both films were 10-12 nm. Patterns of silicides and Si stripe lines were formed on Si substrates by selective-area silicidation using SiO_2 mask (**Fig. 3**). Raman measurements were performed using a UV confocal Raman microscope (Nanofinder 30, Tokyo Instruments) equipped with an Olympus 1.3 numerical aperture (x100) oil immersion micro-objective lens [7]. Spatial resolution is about 150 nm.

Metal S/D MOSFETs were prepared on 10 nm-thick SOI wafers with intrinsic channel concentration, using epitaxial $NiSi_2$ S/D combined with metal/high-k gate stack (**Fig. 5**). Effective Schottky barrier heights of metal S/D for NFET and PFET were adjusted by dopant segregation technique using phosphorus and boron and activation anneal at 600ºC. Electrical characteristics in this study were all examined by 100 nm gate length FETs at temperatures between 233K and 393K.

3. Results and Discussion

Measurement of silicidation induced stress in Si

Raman shifts and calculated tensile stresses for NiSi/Si and $NiSi_2$/Si samples are shown in **Fig. 4(a)**. Considerably large tensile stresses exist in Si areas with maximum stresses 280MPa for NiSi/Si and 100MPa for $NiSi_2$/Si, respectively. This is a favorable situation for the enhancement of NMOS performance.

The FWHM of Raman spectrum is considered to be a measure of disorder in Si crystal caused by stress (**Fig. 4(b)**). In case of the $NiSi_2$/Si sample, the FWHM is settled in a slight increase from the reference and constant across the Si stripe. In contrast, the FWHM of the NiSi/Si sample is very large at around interfaces. A large stress in NiSi/Si system seems to generate a complicated strain distribution at interface. Thus $NiSi_2$ is preferable for metal S/D.

Contrastive temperature dependences of N- and P-FETs

I_D-V_G characteristics of N- and P-FETs with temperature are plotted in **Fig. 6**. V_{TH} decreases and subthreshold swing increases as the temperature increases. Impact of temperatures on drain currents at $|V_D|$=50 mV and $|V_G-V_{TH}|$=0.8V was inspected. Drain currents were normalized by the value at 300K and plotted in **Fig. 7**. Interestingly, a positive correlation with temperature is found in PFET, while a negative correlation with temperature appeared in NFET. Temperature dependences of physical properties responsible for FET performance such as channel mobility and thermionic injection ratio at Schottky junction are considered to be the same for both NFET and PFET in this experiment. A remaining factor is the silicidation induced tensile stress in Si channel which decreases as the temperature increases because of the expansion of silicide region. This change might be the reason of temperature dependences in Fig. 7. Although the change of I_D seems to be too large and a quantitative estimation of stress effect is remaining as a future work, the opposite behaviors of NFET and PFET are not welcomed from the viewpoint of designing a balanced device performance in a wide range of temperature.

Conclusions

Silicidation induces tensile stress into Si channel. It results in the opposite temperature dependences of N- and P-FET performances. Silicidation induced stress might be a crucial issue in metal S/D technology.

Acknowledgements

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Table 1 Physical properties of NiSi, $NiSi_2$, and Si [1-3]. The CTE is an abbreviation of coefficient of thermal expansion coefficient.

	NiSi	$NiSi_2$	Si
Resistivity (μΩ-cm)	10.5-18	34-50	
Crystal structure	Ortho.	Cubic	Cubic
Lattice constants (Å)	*a*=5.175 *b*=3.321 *c*=5.609	5.416	5.430
CTE (x10^{-6}/K)	*a*-axis 42 *b*-axis -43 *c*-axis 34	14.5	2.60
Young's modulus (MPa)	132		130-187

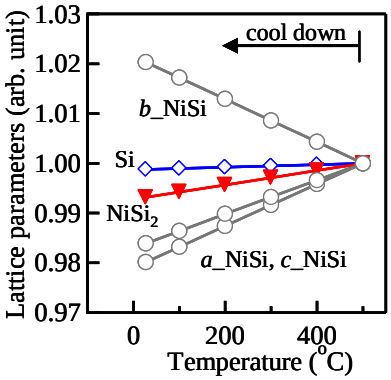

Fig. 2 Variation of lattice parameters with temperature calculated from the CTEs in Table 1. The parameter at silicidation temperature (500ºC) is set as a standard. Upon cooling down, volume mismatch between silicide and silicon enlarges.

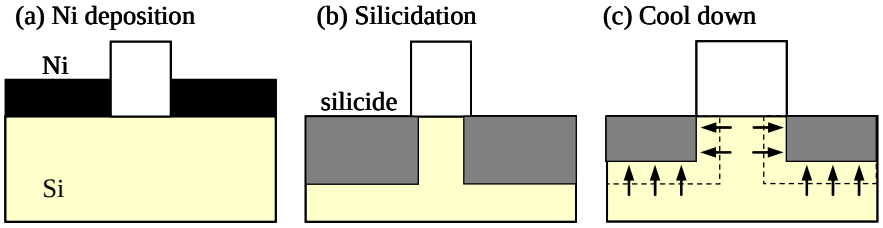

Fig. 1 Illustration of stress generation mechanism by silicidation. (a) Deposition of Ni film. (b) Silicidation and formation of rigid bonding at silicide/silicon interface at 500ºC. (c) Contraction of silicide and generation of stress occurs by cooling down to room temperature.

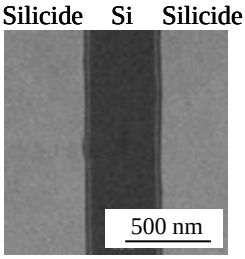

Fig. 3 SEM image of silicide and Si stripe line formed on Si substrate. Raman spectra were measured across the Si stripe.

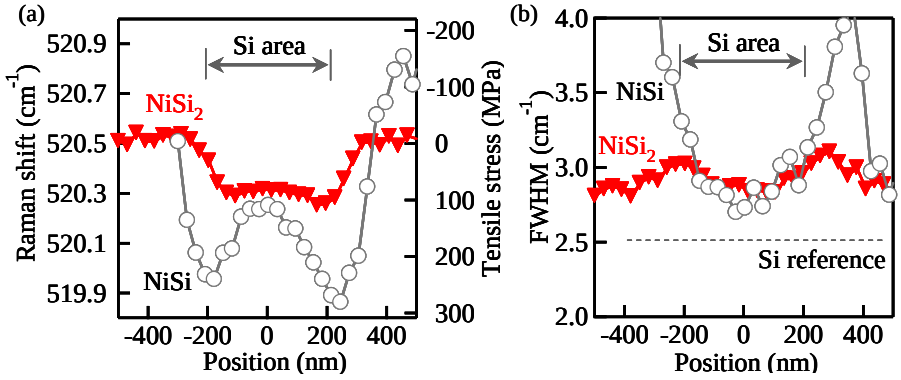

Fig. 4 (a) Raman shifts across the Si stripe for NiSi/Si (open circle) and $NiSi_2$/Si (colsed triangle) samples. The right axes is converted to tensile stress. (b) FWHM of Raman spectra across the Si stripe compared with the 2.5 cm^{-1} for a reference Si substrate.

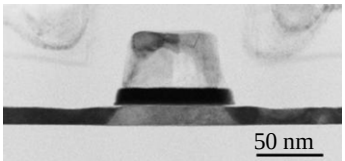

Fig. 5 XTEM image of epitaxial $NiSi_2$ metal S/D SOIFET with metal/high-k gate stack (EOT=1.5 nm).

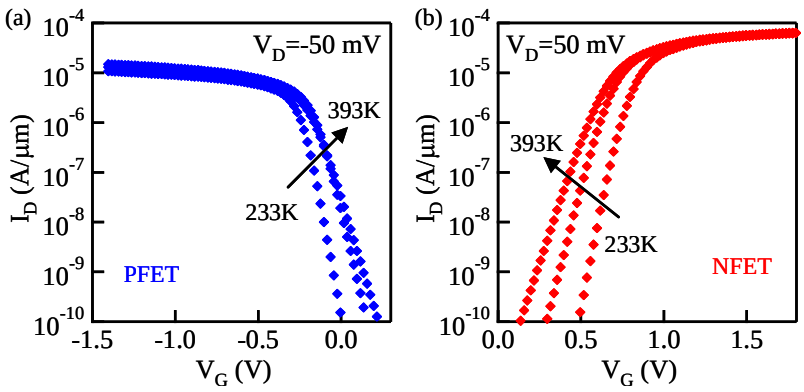

Fig. 6 Temperature dependences (233K, 300K, and 393K) of I_D-V_G ($|V_D|$=50mV) for (a) PMOSFET and (b) NMOSFET with L_G=100 nm.

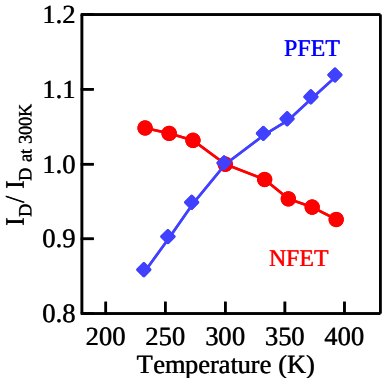

Fig. 7 Normalized I_D ($|V_D|$=50 mV) vs. temperature. I_D were taken at $|V_D|$=50 mV and $|V_G-V_{TH}|$ = 0.8 V for both NFET and PFET, and normalized by the value at 300K.