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Accurate Measurement of Silicide Specific Contact Resistivity by Cross Bridge Kelvin Resistor for 28 nm CMOS technology and Beyond

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1. Introduction

Specific contact resistivity (ρ_c) at interface between silicide and diffusion layer at source/drain electrode is one of major parasitic resistance components of transistors. Accurate measurement of it is strongly required not only for device modeling but also further performance pursuit in development phase. It has been reported that NiPt silicide specific contact resistivity reaches to 1×10^{-8} Ω-cm^2 or less and its extendibility to 22 nm CMOS technology by using the test structure with 20-nm-scale-diameter-silicided area patterned by using electron beam lithography on highly doped diffusion layer with 1-µm-depth on substrate[1]. On the other hand, CBKR (Cross Bridge Kelvin Resistor), that has silicide block layer to create lateral special separation between silicided area and unsilicided area is well-known for ρ_c test structure and has complete compatibility to standard fabrication process, however, in practical, it is difficult to extract ρ_c with high resolution due to parasitic components [2-5]. In this paper, firstly, we've examined resolution of CBKR test structures by utilizing 3-dimensional TCAD (Technology Computer-Aided Design) from viewpoint of extendibility to ρ_c of 10^{-10} Ω-cm^2. In following section, by using these test structures, we've discussed ρ_c achievement in state-of-the-art 28-nm technology [6] in contrast to the value, that the ITRS 2009 Edition [7] stipulates as $\rho_c < 8\times10^{-8}$ Ω-cm^2.

2. Discussion on ρ_c test structure resolution of CBKR

Accuracy examination on CBKR structure was performed by utilizing 3-D TCAD simulation. Conventional CBKR top-down layout has four terminals, two of which are used for constant current flow and other two of which are used for potential difference monitoring (Fig. 1). Cross sectional schematics of A-A' cut in Fig.1 explain that there are silicided areas spatially separated by silicide blocking layers patterned on n$^+$ (or p$^+$) diffusion layer, that were created simultaneously while source-drain diffusion layer formation by 28 nm CMOS technology. It is note that this test structure requires no special or additional process steps to CMOS platform process flow. This is the most advantageous point of CBKR. By using TCAD, distributions of current and potential are simulated for given ρ_c. Extracted ρ_c ($\rho_c=V_m/I$, where V_m is potential difference between two potential monitor electrodes, and I is given constant current.) are plotted against given ρ_c (Fig. 3). It is found that extracted ρ_c starts to show deviation from given ρ_c at approximately 2×10^{-8} Ω-cm^2 with decreasing of given ρ_c. Therefore, as long as this structure is used, it is very difficult to measure 10^{-8} Ω-cm^2 order of ρ_c, which is quite consistent to literatures [2-5]. This saturation of extracted ρ_c is mainly due to potential drop in parasitic components such as silicide layer. In order to eliminate voltage drop within silicide, an additional voltage monitor electrode was formed as shown in Fig. 4. Utilizing this test structure (modified CBKR) , of which top down SEM images after silicide are shown in Fig. 5, it is found that accuracy of extracted ρ_c is extended to level of 10^{-9} Ω-cm^2 as shown in Fig. 6. Still, however, it shows ρ_c saturation at around 10^{-10} Ω-cm^2. To clarify origin of this, simulation under hypothetical condition of 10^{-4} x lower silicide resistivity for elimination of potential drop in silicide, results in no saturation of extracted ρ_c (Fig. 8). Therefore, extracted ρ_c saturation at 10^{-10} Ω-cm^2 is mainly due to potential drop within silicide layer (Fig. 7 (a)). Another deviation component of extracted ρ_c is slight superficial ρ_c lowering compared to given ρ_c as shown in Fig. 6. The root cause is current crowding described by transfer length ($L_t = (\rho_c/\rho_d)^{1/2}$, where ρ_d is diffusion sheet resistance) (Fig. 7 (b)). Even considering deviation between given and extracted ρ_c, it is found that the modified CBKR is able to be used for ρ_c range of 10^{-9} Ω-cm^2 owing to extraction error reduction, that corresponds to 35% error from 260% error of conventional CBKR according to Figs. 3 and 6. This indicates that the modified CBKR is applicable to 28 nm CMOS technology and beyond.

3. Status of achievement of 28-nm technology ρ_c

On 28 nm CMOS technology, actual measured resistance for silicide on n$^+$ and p$^+$ S/D diffusion layers are plotted as a function of inverse of silicided area (Fig. 9). It is achieved that good linearity of data plot and extreme low values of ρ_c with 8.3×10^{-9} +/- 8×10^{-10} Ω-cm^2, 5.3×10^{-9} +/- 1×10^{-9} Ω-cm^2 for n$^+$ and p$^+$ S/D diffusion layers, respectively. Considering error calibration by TCAD discussed in section 2, calibrated ρ_c corresponds to 1.1×10^{-8} +/- 9×10^{-9} Ω-cm^2, 7.8×10^{-9} +/- 1×10^{-9} Ω-cm^2 for n$^+$ and p$^+$ diffusion layers, respectively. To investigate further reduction of ρ_c on n$^+$ diffusion layer, impact of pre-amorphization implantation (PAI) prior to source-drain doping on ρ_c is also examined. PAI helps to reduce 20% of ρ_c. It is speculated that PAI promotes additional n$^+$ dopant activation during annealing process. ITRS requirement for 28 nm node corresponds to 8.0×10^{-8} Ω-cm^2 [7]. It is found that outstanding ρ_c value is realized by 28 nm CMOS technology [6].

4. Conclusions

It is found that modified CBKR has ρ_c measurement accuracy down to 10^{-9} Ω-cm^2 within 35% systematic error that can be calibrated by 3-D TCAD. By using it, it is found that 28 nm CMOS technology realizes ρ_c of 1.1×10^{-8} Ω-cm^2, 7.8×10^{-9} Ω-cm^2 for n$^+$ and p$^+$ source/drain diffusion layers, respectively, which are enough to satisfy ITRS 2009 requirements as ρ_c less than 8×10^{-8} Ω-cm^2 [7].

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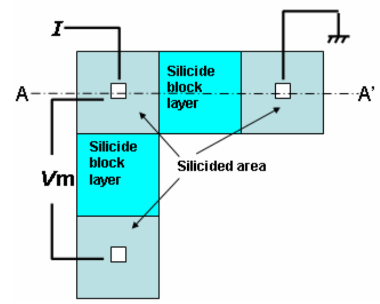


Fig.1 Topdown schematic layout of conventional CBKR test structure simulated by 3-D TCAD.

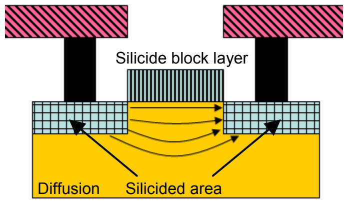


Fig.2 Cross sectional schematics of A-A' cut of conventional CBKR shown in Fig. 1.

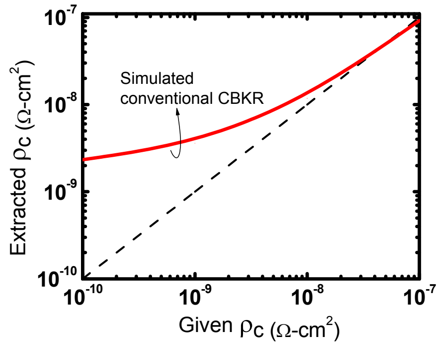


Fig.3 Extracted ρ_c simulated by 3-D TCAD for conventional CBKR.

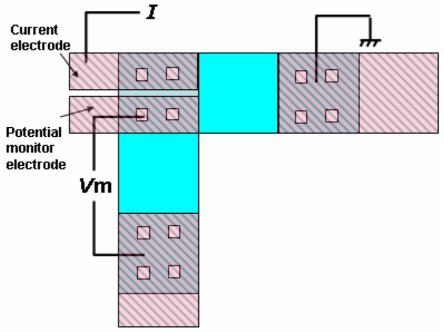


Fig.4 Topdown schematic layout of CBKR test structure with additional probe for potential monitoring simulated by 3-D TCAD.

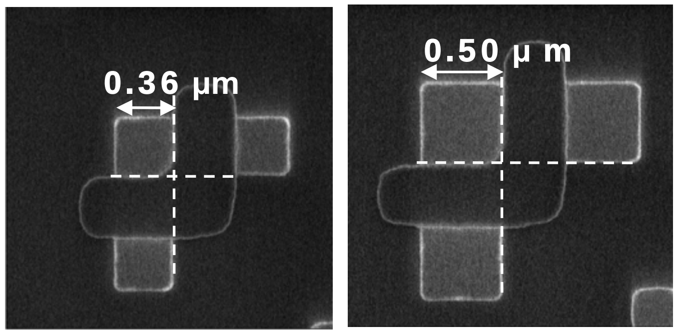


Fig.5 Topdown SEM images for CBKR test structure that just received silicide process.

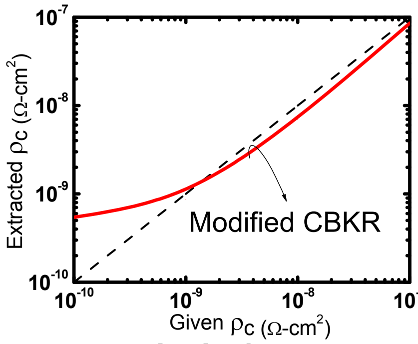
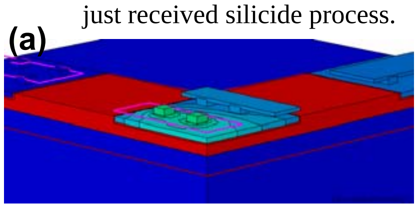


Fig.6 Simulated ρ_c by using CBKR with additional potential monitoring probe. Its resolution has been improved to 10^{-9} Ω-cm^2 range.



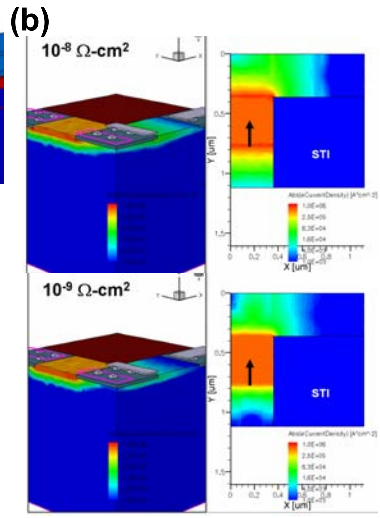


Fig.7 (a) Simulated potential distribution in silicide layer in case of 20μΩ-cm silicide resistivity and ρ_c of 10^{-9} Ω-cm^2. (b) Current density distribution comparison between 10^{-8} Ω-cm^2 and 10^{-9} Ω-cm^2. Lower ρ_c sample shows current crowding near silicide block layer.

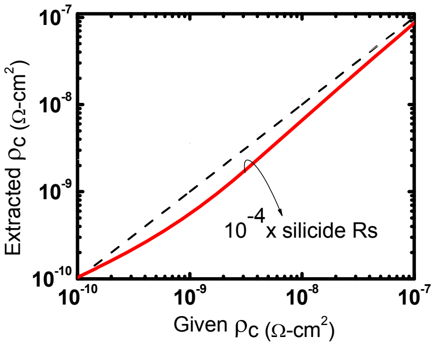


Fig.8 Simulated ρ_c by using CBKR with additional potential monitoring probe under the assumption of silicide with 10^{-4} x lower resistivity.

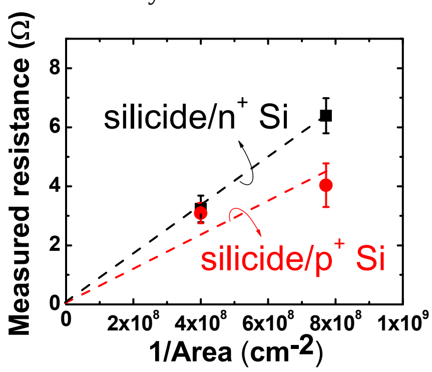


Fig. 9 Area dependence of measured resistance on samples for silicide/n$^+$ diffusion layer and silicide/p$^+$ diffusion layer.

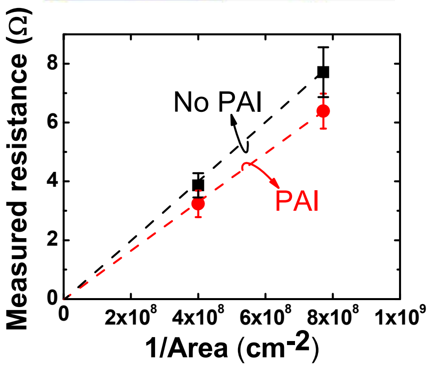


Fig.10 Area dependence of measured resistance on samples with PAI and without PAI.