Extended Abstracts of the 2010 International Conference on Solid State Devices and Materials, Tokyo, 2010, pp998-999

Measurements of Electrostatic Potential Across p-n Junctions on Oxidized Si Surfaces by Scanning Multi-Mode Tunneling Spectroscopy

Leonid Bolotov, Tetsuya Tada, Masanori Iitake, Masayasu Nishizawa and Toshihiko Kanayama

Nanodevice Innovation Research Center, AIST, 1-1-1, Higashi, Tsukuba, Ibaraki 305-8562, Japan
Phone: +81-29-849-1634 E-mail: bolotov.leonid@aist.go.jp

1. Introduction

Nanoscale potential fluctuations in semiconductor devices by interface charges and impurity atoms can lead to deteriorating the performance of small devices. Thus, characterization of the electrostatic potential and sub-surface charge distribution in modern Si devices at an atomic scale is an essential issue. While images of individual dopant atoms were demonstrated on ideal, atomically flat Si surfaces by probe microscopy techniques,[1-3] quantitative measurements of potential profiles on device cross sections are still significant challenges.

In this paper, we investigated variation of contact potential difference (CPD) voltage across p-n junctions on oxygen-passivated Si(110) surfaces by a scanning multi-mode tunneling spectroscopy, which can detect tip-surface force simultaneously with the tunneling current. Here, we develop a scanning tunneling microscope (STM) mode, in which the tip-sample gap is adjusted to reduce short-range interactions by maintaining the tunneling current at a specified bias voltage, thus, improving the sensitivity to electrostatic force. We show that the CPD voltage, derived from force gradient - bias voltage curves, agrees with the expected build-in potential across the p-n junction when the optimal tip-sample gap is maintained. The CPD voltage showed a standard deviation of ~30 mV on atomically flat terraces. Larger fluctuations were observed arising from structural and charge variations on the surface.

2. Results and Discussion

Principle of CPD measurement in STM mode

For passivated Si surfaces, the applied voltage V_0 is shared between the vacuum gap (V_{gap}) and the band bending region (V_{bb}) beneath the surface in the constant tunneling current mode as illustrated in Fig. 1(a).[4] For the applied voltage V_0, the electrostatic force gradient between the probe tip and the sample is expressed as:

$$\frac{\partial F}{\partial z} = -\frac{1}{2}\left(V_0 - CPD\right)^2 \frac{\partial^2 C}{\partial z^2} \propto \Delta f \qquad (1)$$

where C is the effective tip-sample capacitance, and Z is the tip-sample gap. Since a CPD voltage originates from the difference in work function of the probe tip (ϕ_M) and the Fermi energy of underlying Si (E_F), the minimum of the force gradient occurs when

$$V_0 = CPD = \left(E_F - \phi_M\right) \qquad (2)$$

as illustrated in Fig.1 (b). Thus, it is an effective method to monitor variation of the Fermi energy across p-n junctions.

In our measurements, the force gradient is detected as a shift of the resonance frequency (Δf) of a quartz oscillator,[2] when a sharp metal probe attached to the oscillator vibrates normal to the surface with amplitude of 0.3 nm at a resonance frequency of ~1 MHz. A (Δf - V_0) spectrum was measured by sweeping the bias voltage (V_0) while holding the mean gap width. The CPD voltage was derived from a fit of the spectrum to Eq.1 as illustrated in Fig.2 (b).

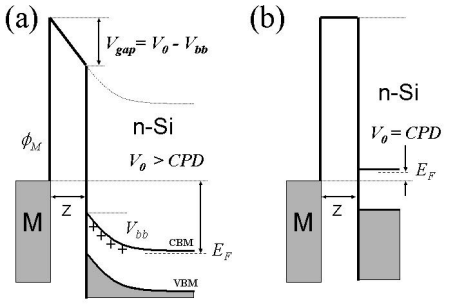

Fig. 1 Energy diagrams of STM junction between a metal probe (M) and n-Si under a bias voltage V_0 corresponding to the STM mode (a) and a minimum of the force gradient (b).

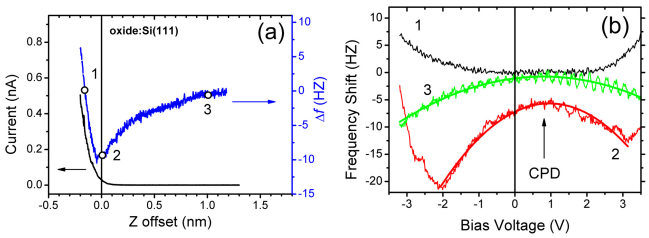

Fig. 2 Current-Z and Δf -Z spectra under V_0=2 V (a) and Δf -V_0 spectra taken at different gap distances (b) measured on an oxidized Si(111) surface. Lines are fits to Eq.1.

Figure 2 shows adjustment of the tip-sample gap to enhance sensitivity to electrostatic force while minimizing short-range chemical interaction. When the gap maintained a mean tunneling current of 30 pA at a bias voltage of 2.0 V, attractive electrostatic force caused the largest negative shift of the frequency and prevailed over short-range repulsive forces as seen in Fig. 2(a). At the optimum distance the steepest curvature of the Δf - V_0 spectrum was observed in Fig. 2(b), curve 2. At a smaller gap, curve 1, the repulsive forces obstructed the CPD measurements.

CPD measurements on p-n junction cross sections

Samples with p-n junctions were prepared according to the normal CMOS fabrication process described in Ref. [5] where antimony ions were implanted to a peak concentration of ~5x10^{19} /cm^3 into a p-Si(001) substrate (1x10^{17} /cm^3,

boron). Cross-sectional surfaces were prepared by polishing to expose (110) surfaces, and were passivated by ultra-thin oxide layers grown at ~600°C under an O_2 pressure of $3x10^{-3}$ Pa following etch-cleaning in HF:HCl (1:19). [6] For comparison, samples with atomically flat terraces were prepared from a Si(111) wafer by flash-anneal to ~1200°C in an ultra-high vacuum (~4×10^{-9} Pa) prior to oxidation. To reduce trap density in the oxide, the samples were annealed in a mixture of N_2 : H_2 (95%: 5%) at 450 C and a pressure of ~1 Pa for 30 min. The measurements were done in vacuum at room temperature and the dark conditions.

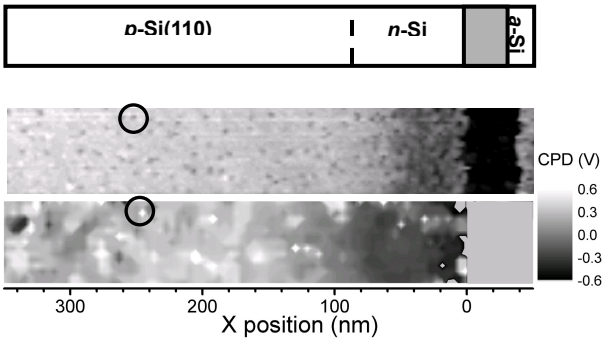

Fig. 3 Sample structure (top), STM topograph (middle) and corresponding map of the CPD voltage (bottom) for the oxidized cross section of Si p-n junctions. The grayscale is 4 nm. The cross section area is 400 x 70 nm^2. Circles outline a surface defect.

Figure 3 shows typical STM topograph of the p-n junction surface acquired with a mean tunneling current of 30 pA at 2.0 V. A black trench used to navigate to the implanted region edge at X = 0 nm. Black spots are small surface holes of ~1 nm in depth.

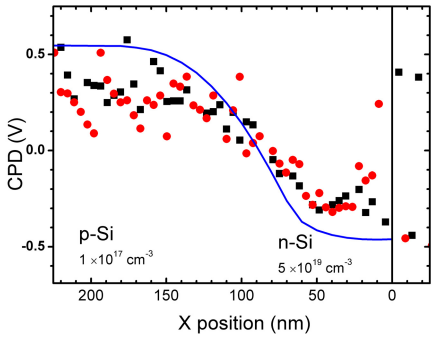

Fig. 4 Line profiles (symbols) of the CPD voltage across the p-n junction, and a simulated profile of the build-in potential (line).

For the optimized gap a CPD map was obtained by fitting an array of the spectra taken in the surface area with a spacing of 4 nm. The CPD map in Fig.3 and line profiles in Fig.4 show gradual change in the CPD voltage from -0.35 V in n-Si at a depth of 50 nm to about +0.40 V in p-Si at 140 nm. Similar profiles were obtained with 3 different probe tips. The measured CPD profiles well agree with the build-in potential profile simulated for a dopant distribution derived from SIMS data and ϕ_M = 4.5 eV. The deviation of the CPD voltage from the simulated values in n-Si is attributed to contribution of long-range electrostatic forces between the STM probe and neighboring p-Si regions, so called the patch potential effect.[7]

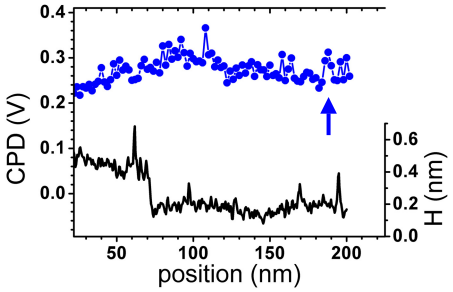

Fig. 5 Line profiles of the CPD voltage (symbols) and the height (line) as a function of position on the oxidized Si(111) surface.

Origin of CPD fluctuations on atomically flat terraces

To elucidate origin of fluctuations in the CPD voltage seen in Figs. 3 and 4, the CPD voltages were measured on surfaces with atomically flat terraces. Figure 5 shows a line profile of CPD voltage measured with a spacing of 2 nm along the atomic terrace on the oxidized Si(111) surface. A small structure of ~4 nm in size is resolved in the CPD profile at ~190 nm. We see in addition to a standard deviation of 30 mV, 'spikes' of ~80 mV and a variation of ~100 mV in the CPD voltage across the atomic step due to dipole moments at the surface steps.[3] These account for scattering of the CPD voltage in the p-n junction region at a position of 20 - 140 nm in Fig.4. Large fluctuations in the CPD value correlate with some surface defects as outlined by circles in Fig.3, suggesting the effect of variation in gap width and oxide thickness on the effective probe-sample interaction.

3. Conclusions

Measurements of the CPD voltage in STM mode was demonstrated on oxidized Si(110) surfaces of p-n junction cross sections. The observed CPD voltage agrees with the expected build-in potential across the p-n junction. Scattering of the CPD voltage is attributed in part to the effects of the surface morphology. The results show the ability of the CPD measurement for local characterization of small CMOS and nanowires devices.

Acknowledgements

The work was supported by NEDO. A part of this work was conducted at the Nano-Processing Facility, supported by IBEC Innovation Platform, AIST.

References

[1] M. Nishizawa, et al., Appl. Phys. Lett. **90** (2007) 122118.
[2] M. Tabe et al., Thin Solid Films **518** (2010) S38.
[3] S. Kitamura, M. Iwatsuki, Appl. Phys. Lett. **72** (1998) 3154.
[4] M. Weimer, et al., Phys. Rev. B **39** (1989) 5572.
[5] H. Fukutome, et al., Jpn. J. Appl. Phys. **43** (2004) 1729.
[6] L. Bolotov, et al., J. Vac. Sci. Technol. B **26** (2008) 415.
[7] N.A. Burnham et al., PRL **69** (1992) 144.