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Contributions of Interface-Trap and Minority-Carrier Responses to C-V characteristics of Al_2O_3/InGaAs Capacitors

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1. Introduction

Development of high mobility channels is one of the key issues to improve the performances of the CMOS devices in the post-scaling generations. [1)] InGaAs is a promising n-channel material which potentially surpasses the-state-of-the-art strain-Si technology. [2,3)] Suppressing the interface traps at the oxide/InGaAs interfaces is important for improving the device characteristics. For this purpose, appropriate electrical characterization for the interface trap response is required. However, since the bandgap of InGaAs is relatively small (0.74 eV for In concentration of 53 %), the minority carrier response hampers the conventional room-temperature measurement of the interface traps.[4)] Actually, room-temperature ***C-V*** curves of an ALD-Al_2O_3/InGaAs MOS capacitor show inversion capacitance at low frequency (100-1k Hz), as shown in Fig. 1. Low-temperature measurement is usually used to suppress such minority carrier responses.[5)] However, there was no clear evidence for the detection of the true interface trap responses by the low-temperature measurements for the oxide/InGaAs MOS structures.

In this study, we examine the interface-trap and minority-carrier responses in the capacitance and conductance for the Al_2O_3/InGaAs MOS capacitors by using variable temperature measurements.

2. Experimental

A MIS capacitor was fabricated on the $In_{0.53}Ga_{0.47}As$(100) layer that was 1 μm in thickness and heteroepitaxially grown on an InP(100) wafer by MOCVD. The InGaAs surface was treated in an $(NH_4)_2S$ solution for 10 min at room temperature. The sample was subsequently rinsed in flowing deionized water followed by drying the surface using an N_2 blowgun. After the surface treatment, an Al_2O_3 layer was grown by atomic layer deposition (ALD) using $Al(CH_3)_3$ and H_2O at 250°C. The sample underwent post deposition annealing (PDA) at 400°C in vacuum for 2 min. Gold gate electrodes with the area of $3.14x10^{-4}$ cm^2 were evaporated on Al_2O_3 using a stencil mask immediately after the Al_2O_3 deposition. The Cr/Au back contact metal was finally formed.

3. Results and Discussion

The *C*-V_g curves measured at -50°C show suppressed inversion capacitance as shown in Fig. 2. The humps observed near Vg= 0V possibly include the responses of the interface trap states and the minority carriers generation in the substrate. The G_p/ω contour map in Fig. 3 shows an obvious ridge structure. Although the interface trap densities are often determined from such G_p/ω data, the effects of the minority carrier responses must be examined. In the following, we discuss this issue carefully.

The interface-trap and minority-carrier responses can be separated by analyzing the temperature dependence of G_p. Figure 4 shows the *C*-V_g data taken at different temperatures. The associated G_p-V_g data are also shown in Fig. 5. We estimated the conductance component G_p by assuming a simple three terminal model. [5-7)] The G_p peak becomes smaller with decreasing the temperature. Figure 6 shows the Arrhenius plots of G_p at 5k Hz. For V_g=-2.0 V, two temperature regions with different activation energies of 0.61 eV and 0.32 eV can be recognized. It is well known that the rate-limiting step for the minority carrier supply depends on the temperature, *i.e.*, minority carrier generation in the depletion region [$G_{p\_inv} \sim exp(-E_g/2kT)$] and minority carrier diffusion from the bulk region [$G_{p\_inv} \sim exp(-E_g/kT)$]. Since the energy gap of $In_{0.53}Ga_{0.47}As$ is 0.74 eV, the observed activation energies (0.61 and 0.32 eV) for V_g=-2.0 V can be explained by the above mechanisms. The activation energies in both temperature regions decrease with decreasing V_g. These results indicate that the carrier generation mechanism is changed from minority carrier diffusion to interface-trap responses with decreasing V_g. At the lower frequency of 100 Hz, the dependences on the temperature and V_g were essentially the same as those at 5 kHz, except for the absence of the temperature region with activation energy of $E_g/2$ (Fig. 7).

Figure 8 summarizes the variation of the activation energy with changing V_g. E_a is nearly constant for V_g ~ -2 V, which implies that the surface is inverted under this bias condition. Meanwhile, E_a decreases with increasing V_g for V_g > -1.5 V. It was reported that the activation energy for the interface-trap response depends on the surface potential [$G_p \sim exp(\Phi_s)$], because an energy level of the responding interface traps is a function of surface potential, Φ_s.[6)] Thus, we can safely say that the interface traps are responsible for the G_p/ω ridge structure measured at -50°C [Fig. 3]. The surface is depleted under the V_g conditions where the ridge structure is observed in Fig.3 (-0.5 V < V_g < 0 V). The minimum interface state density was estimated to be ~10^{11} $cm^{-2}eV^{-1}$ using the equation of D_{it}= 2 $G_p^{max}/\omega q$. However, the actual D_{it} would be higher (~10^{12} $cm^{-2}eV^{-1}$) if the surface potential fluctuation is taken into account. We note that the slopes of the E_a-V_g plots are much smaller than that for the ideal Φ_s-V_g relation, which means that the Fermi level modulation near the midgap is impeded by the interface traps.

4. Conclusion

We clarified the contribution of minority-carrier response to the *C-V* and conductance characteristics of ALD-Al_2O_3/InGaAs MIS capacitor using the temperature-dependent measurement. As a result, we found that the G_p/ω ridge structure measured at -50°C is mainly composed of the interface-trap responses.

Acknowledgment

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References

1) S. Takagi et al.,:*IEEE Trans. Electron Device* **55** (2008) 21.
2) Y. Xuan et al.,:*IEEE IEDM* 637 (2007).
3) H. Ishii et al.,:*Appl. Phys. Exp* **2** (2009) 121101.
4) K. Marten, C et al.,:*IEEE Trans. Electron Device* **55** 2 (2008) 547.
5) A. Dimoulas et al.,:Microelectronic Engineering, 80 (2005) 34-37.
6) E. H. Nicollian and J. R. Brews, MOS Physics and Technology (Wiley, New York, 1982).
7) N. Miyata et al.,:Applied Physics Express **3** (2010) 035701.

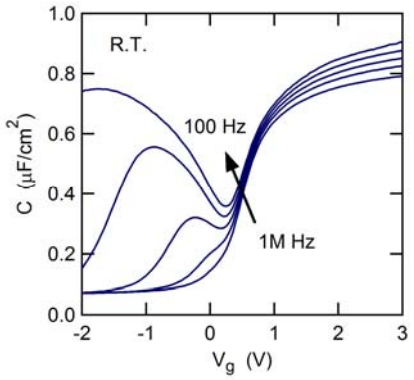

Fig. 1. Capacitance voltage characteristics with various frequencies at room temperature.

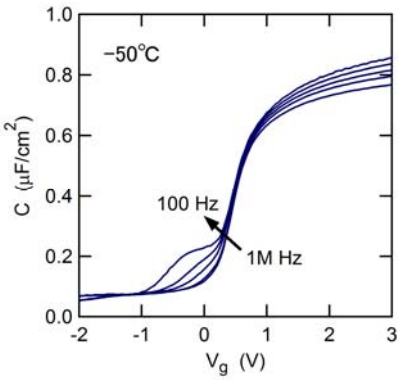

Fig. 2 Frequency dependence of capacitance voltage curves at -50℃.

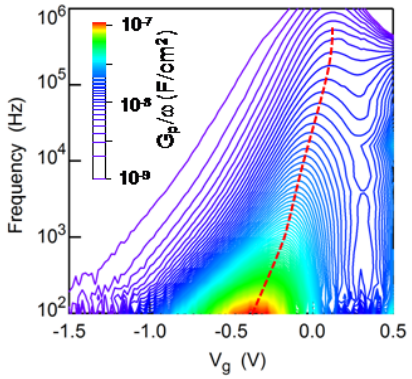

Fig. 3 Frequency dependence of conductance (G_p/ω) at -50℃.

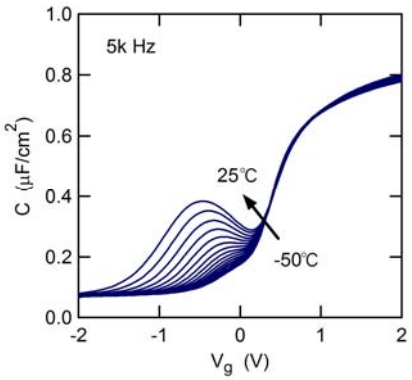

Fig. 4 Temperature dependence of capacitance voltage curves at 5k Hz.

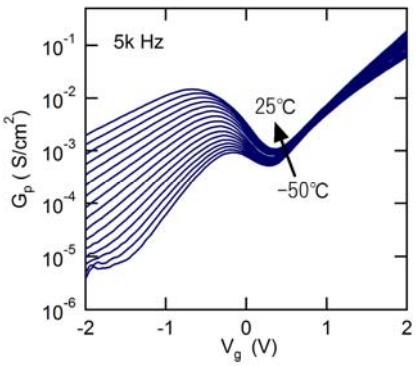

Fig. 5 Temperature dependence of conductance (G_p) at 5k Hz.

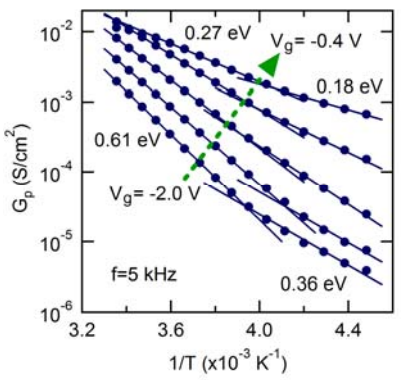

Fig. 6 Arrhenius plot for conductance (G_p) at 5k Hz.

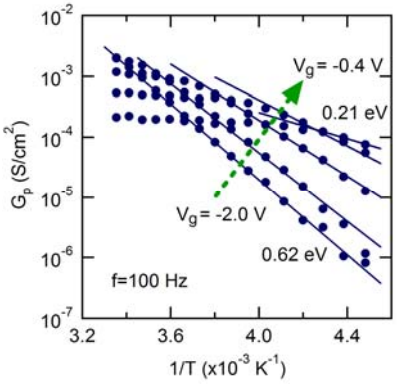

Fig. 7 Arrhenius plot for conductance (G_p) at 5k Hz and 100 Hz.

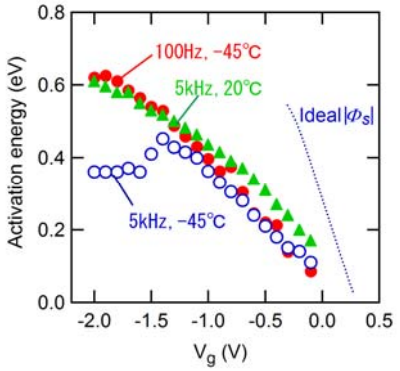

Fig. 8. Activation energy as a function of gate voltage.