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New Insights into Flicker Noise Improvement Mechanism Using Random Telegraph Signal Technique

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Abstract

The conventional flicker (1/f) noise improvement approaches such as fluorine incorporation and hydrogen sintering are interpreted, for the first time, by detecting the border traps using the random telegraph signal (RTS) technique. The results show that the improvement in low frequency noise by F-incorporation can be mainly attributed to the relaxed trap-to-carrier influence. On contrary, the H_2-annealing is found to improve the low frequency noise by the reduced trap density.

Introduction

The 1/f noise in MOSFETs has been studied for several decades due to its significant influence on the high frequency performance of the analog circuits [1]. The 1/f noise has also been regarded as one of the important techniques for the border traps characterization [2, 3]. Border traps will be increasingly important in the ultra-thin gate oxide where all the oxide traps may act as border traps on the conventional time scale of the noise measurement (Fig. 1). F-incorporation is known as an effective way to improve the conventional SiO2 gate dielectric integrity, and both the reliability and 1/f noise [4] improvement have been reported. Moreover, H_2-sintering is found to influence the electrical performance of MOS devices and improve the interface quality [5]. In this work, we report a detailed characterization of border traps in F-incorporated and H_2-annealed SiON gate dielectric using the drain current-RTS (I_d-RTS) technique [6] to investigate the mechanisms responsible for the 1/f noise improvement.

Device Fabrication

The 65nm technology was used for devices fabrication. Three categories of devices were prepared. The first one is F-incorporated device fabricated by receiving additional F-implant step. The second one is H_2-annealed device fabricated by subjecting to additional low temperature H_2 sintering step. And the third one is the control device. In an attempt to be helpful for RTS measurement, devices with small channel area were prepared. All devices have SiON gate dielectric with EOT=2.6nm.

Results and Discussion

Several kinds of applications had been reported for RTS technique in the past decades. Table-I summarizes the equations [1] for traps characterization, and the definitions of parameters can be found in Fig. 2-3. Firstly, Fig. 4 shows the measured I_d-RTS of nFET with small area (L=0.06um, W=1um) under constant V_d and varying V_g. According to the trend of t_{on} versus V_g, one can determine the type of detected border trap as acceptor-like trap or donor-like trap. Simultaneously, the correlation between t_{on} and t_{off} to mean capture t_c and mean emission time t_e can be decided as well. For instance, a decreasing t_{on} with the increasing V_g in Fig. 5 exhibits that the detected border trap is an acceptor-like trap, and the mean capture (emission) time t_c (t_e) can be correlated to t_{on} (t_{off}). Secondly, in the plot of $\ln(t_c/t_e)$ versus V_g (Fig. 6), the fitted slope can be used to extract the depth of the detected border trap from the dielectric/substrate interface (x_T). Thirdly, the location of detected trap along the channel (y_T) can be determined by I_d-RTS along with changing the polarity of source and drain. The different surface potential under forward- and reverse-mode operation can be utilized to determine the trap location in the longitudinal direction (Fig. 7). Fourthly, the I_d-RTS measurement under varying temperature allows one to extract the capture (emission) activation energy, E_c (E_e), of the detected trap (Fig. 8). Finally, the I_d-RTS amplitude has also been reported to reveal the valuable information [7]. The screened scattering coefficient (α) is a key parameter in the reported unified 1/f noise model [8] and can be extracted from the I_d-RTS amplitude using equation (4) in Table-I.

Two mechanisms may be solely or jointly responsible for the 1/f noise improvement. The one is the reduced trap density, and the other is the relaxed trap-to-carrier influence. Fig. 9 shows an obvious improvement in low frequency noise is achieved by F incorporation. To distinguish the mechanism, Fig. 10 compares the mapping results where the location of die with digitized I_d-RTS is highlighted. No obviously difference in the die number implies that the F incorporation does not help to reduce the border trap density. Instead, the noticeable lower (~0.5X) average I_d-RTS amplitude ($<\Delta I_d>$) in F-incorporated device reveals that the 1/f noise improvement can be attributed to the relaxed trap-to-carrier influence which is usually interpreted in terms of number fluctuation and/or mobility fluctuation [9, 10].

Fig. 11 shows the 1/f noise performance of control and H_2-annealed devices. Similarly, the border trap density and the trap-to-carrier influence are evaluated. In Fig. 12, for H_2-annealed wafer, a remarkable increase (~2X) in the number of die with digitized RTS reveals that the border trap density is effectively reduced. The lower trap density enhances the probability of probing a single trap for a given device channel area. It is suspected that the Hydrogen passivation can neutralize not only the interface traps but also the border traps. It is worth to note that the average I_d-RTS amplitudes between control and H_2-annleled devices are comparable. Differing from the case with F incorporation, the H_2 sintering has no obvious effect on relaxing the trap-to-carrier influence as can be observed from the distribution of ΔI_d shown in Fig. 13.

Conclusion

For the first time, the detection of border traps using RTS technique is applied to interpret the mechanisms responsible for the low-frequency-noise improvement. The relaxed trap-to-carrier influence can be observed in devices with F incorporation. On contrary, the reduced trap density is found in devices with H_2 sintering.

Reference

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(1): $\ln\left(\frac{t_c}{t_e}\right)=\frac{E_T-E_F}{kT}=\frac{-1}{kT}\left[\left(E_{Cox}-E_T\right)-\left(E_C-E_F\right)-\Phi_0+qj_s+q\frac{x_T}{t_{ox}}\left(V_{gs}-V_{fb}-j_s\right)\right]$

(2): $\ln\frac{\left(t_c/t_e\right)_{F\_Max}}{\left(t_c/t_e\right)_{R\_Max}}=\frac{q}{kT}\frac{x_T}{t_{ox}}\left[\frac{y_T}{L}V_{ds,F\_Max}-\left(1-\frac{y_T}{L}\right)V_{ds,R\_Max}\right]$

(3): $t_c=\frac{\exp\left(\Delta E_c/kT\right)}{I_d\cdot T\cdot s_0\cdot c}\qquad t_e=\frac{\exp\left(\Delta E_e/kT\right)}{T^2\cdot s_0\cdot h}$

(4): $\frac{\Delta I_d}{I_d}=\frac{\Delta N}{N}\pm\frac{\Delta m}{m}=-\frac{1}{W_{eff}L_{eff}}\left(\frac{1}{N}\pm am\right)$

TABLE-1 Equations for border trap characterization used in this work.

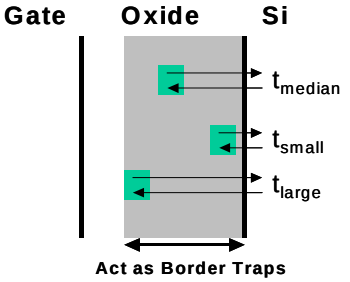

Fig. 1. Illustration of border traps in gate dielectric. The boundary depends on the probing time scale of measurement. For ultra-thin oxide, the shadow region may occupy the whole oxide.

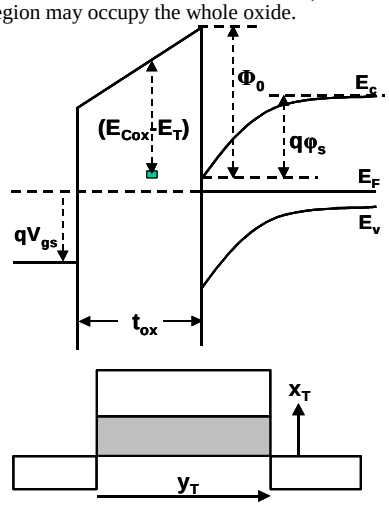

Fig. 2. Parameters definition in energy space (up) and spatial space (down).

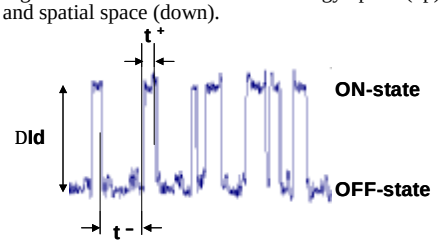

Fig. 3. Parameter definition in I_d-RTS. Note that t_{on} and t_{off} can be derived from the mean value of t^+ and t^-, respectively.

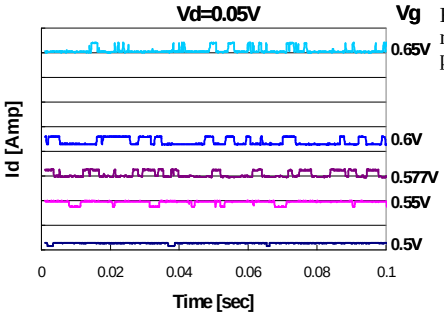

Fig. 4. Measured I_d-RTS under constant V_d and varying V_g for device with small channel area (L=0.06um, W=1um).

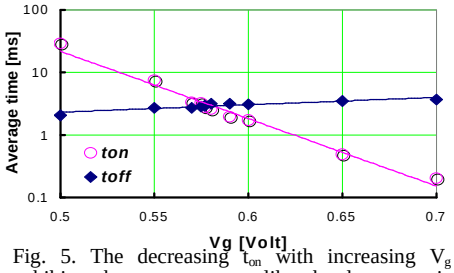

Fig. 5. The decreasing t_{on} with increasing V_g exhibits that an acceptor-like border trap is detected. And one can correlate t_{on} and t_{off} to t_c and t_e, respectively.

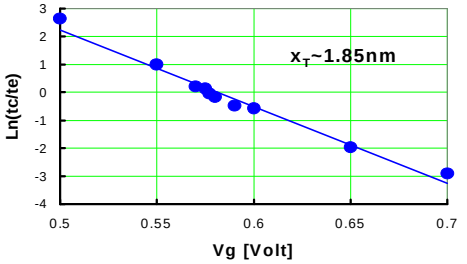

Fig. 6. According to equation (1), the depth of detected trap can be obtained from the slope of $\ln(t_c/t_e)$ vs. V_g.

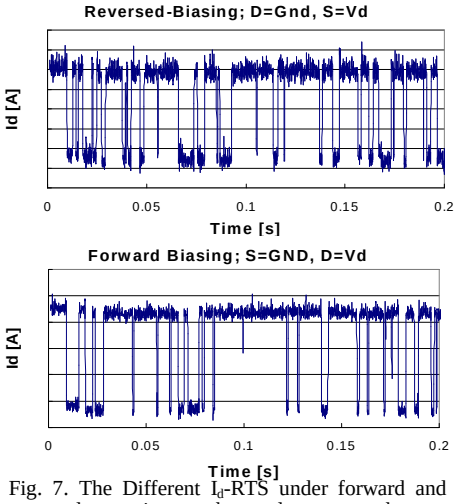

Fig. 7. The Different I_d-RTS under forward and reversed operation can be used to extract the trap position along the channel by equation (2).

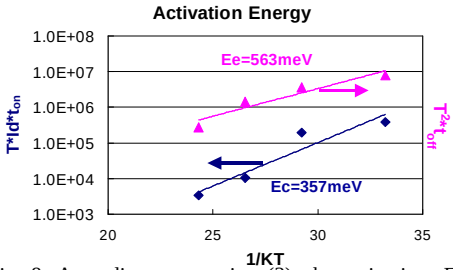

Fig. 8. According to equation (3), the activation energies of detected trap can be extracted.

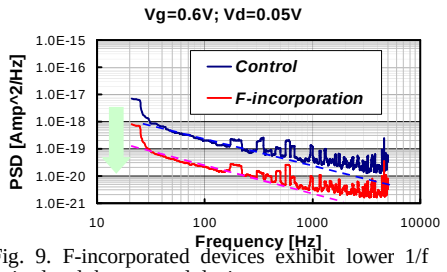

Fig. 9. F-incorporated devices exhibit lower 1/f noise level than control devices.

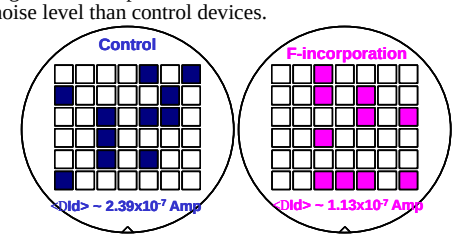

Fig. 10. The number of die with digitized I_d-RTS in F-incorporated wafer is comparable with that in the control wafer.

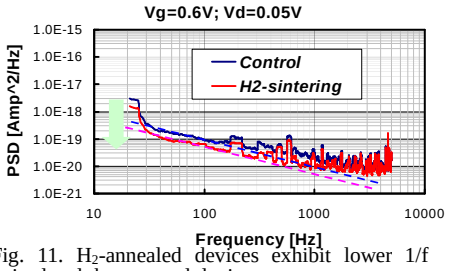

Fig. 11. H_2-annealed devices exhibit lower 1/f noise level than control devices.

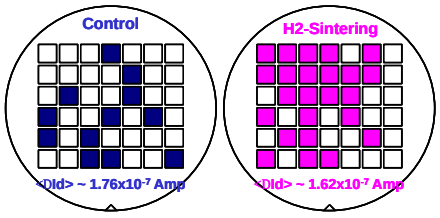

Fig. 12. The number of die with digitized I_d-RTS in H_2-annealed wafer is more than that in the control wafer.

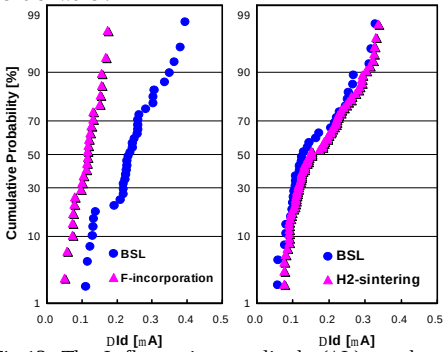

Fig.13. The I_d-fluctuation amplitude (ΔI_d) can be effectively suppressed by F incorporation.