Impact of Transistor Layout Configuration on Current Drive Performance in (100)<110> and (100)<100> SiGe channel pMOSFETs: Comparative Study to Si channel

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Abstract
Carrier mobility modulation by transistor layout configuration in Si and SiGe channel pMOSFETs is systematically studied for (100) surface channel. Hole mobility in SiGe channel by narrowing the channel width, however, hole mobility is deteriorated in <110> channel SiGe pMOSFET when gate length is sufficiently shorter than W. It is found that the biaxial compressive stress, caused by SiGe channel, is a possible parameter which could be used by changing the transistor geometry. Considering the higher hole mobility and affirmative junction leakage current even at 398 K, the optimized channel material and channel direction should be (100)<100> SiGe for the short and narrow channel pMOSFET in the future LSI towards 20 nm node and beyond.

Introduction
In recent years, pMOSFETs fabricated on (110) surface Si substrate 1) or on Ge substrate 2) have attracted much attention, because of the higher hole mobility than that in (100) surface Si channel. These technologies, however, have several drawbacks for CMOS applications, e.g. the smaller electron mobility in nMOSFETs on (110) surface which should be avoided with Direct Substrate Bonded (DSB) technology 3), or higher junction leakage current at high temperature which is due to the narrow band-gap in Ge MOSFET. Therefore, the practical solution for advanced CMOS integration could be the combination of (100) surface Si channel for nMOSFET and SiGe channel for pMOSFET.

This paper discusses the comparison of (100) surface Si and various channel direction of SiGe channel pMOSFETs to clarify the advantages in SiGe channel for LSI application. In previous work, the dependence of channel direction on current drive has been reported in SiGe channel pMOSFETs 4). In this work, much more systematic and detailed study has been performed for (100) surface Si and SiGe channel pMOSFETs to see the impacts of channel materials, device geometries and current drive configuration on hole mobility. Device dimensions were miniaturized down to 32 nm node and beyond.

Device Fabrication
In this work, pMOSFETs down to 25 nm gate length with SiGe channel is fabricated by conventional CMOS compatible processes. SiGe channel were deposited by selective epitaxial growth after finished STI formation, in which Ge concentration was less than 50%. Non-stressed capping liner layer was deposited after gate formation and Source/Drain formation with silicidation. Minimum channel width was 200 nm for fabricated pMOSFET.

Results and Discussion
(1) Phonon scattering limited mobility and junction leakage current:
In most of the previous studies, the operating temperature condition for SiGe channel pMOSFETs has been limited to room temperature. Considering the realistic LSI operation, however, the device should be able to work in higher temperature. In this study, the dependence of phonon scattering on mobility and junction leakage are investigated in more wider temperature range. Figure 1 shows the temperature dependence of the peak mobility in long and wide channel Si and SiGe pMOSFETs from 245 K to 398 K. Hole mobility in SiGe pMOSFET always exceeds that in Si pMOSFET, even at the phonon scattering dominated region. Figure 4 shows the channel width dependence of on-resistance $R_{on}$ in pMOSFET, which relates to the hole mobility. In long $L_g$, but narrower $W$ case, however, $R_{on}$ in <110> channel is much smaller than that in <100> channel in SiGe pMOSFET. These are several of potential reasons for this phenomenon; (a) mobility enhancement by stress relaxation in transverse direction, (b) the facet formation, or (c) the difference in stress from STI. In this case, the length of the facet region was confirmed to be less than 20 nm in both devices by TEM analysis. In terms of (c), the difference in stress from SiGe will be also ignored both for <110> and <100> channels, because relatively small $W$ dependence in mobility has been observed in <110> and <100> Si channels, even with same STI process formation (Fig. 4). Therefore, the hole mobility in narrow $W$ device is affected by uniaxial compressive stress along with longitudinal direction, reducing the contribution of transverse direction. In addition, hole mobility in <110> direction has much larger sensitivity for longitudinal stress compared to <100> direction in SiGe channel.

(2) Channel Width Dependent Hole Mobility in SiGe at Long Channel:
Hole mobility in SiGe pMOSFET was investigated in detail for long and wide channel device. Figure 3 compares the $\mu_{phonon}$-like $\mu(E_F)$ curves for each channel, respectively. It shows almost no major difference between them, on the contrary to the results in Ref. 4. In this case, both pMOSFETs might be operating under the same channel stress, because the channel areas are large enough to have same biaxial stress. Figure 4 shows the channel width dependence of on-resistance $R_{on}$ in pMOSFET, which relates to the hole mobility. In long $L_g$, but narrower $W$ case, however, $R_{on}$ in <110> channel is much smaller than that in <100> channel in SiGe pMOSFET. These are several of potential reasons for this phenomenon; (a) mobility enhancement by stress relaxation in transverse direction, (b) the facet formation, or (c) the difference in stress from STI. In this case, the length of the facet region was confirmed to be less than 20 nm in both devices by TEM analysis. In terms of (c), the difference in stress from SiGe will be also ignored both for <110> and <100> channels, because relatively small $W$ dependence in mobility has been observed in <110> and <100> Si channels, even with same STI process formation (Fig. 4). Therefore, the hole mobility in narrow $W$ device is affected by uniaxial compressive stress along with longitudinal direction, reducing the contribution of transverse direction. In addition, hole mobility in <110> direction has much larger sensitivity for longitudinal stress compared to <100> direction in SiGe channel.

(3) Hole Mobility in Short and Narrow SiGe Channel:
Next, hole mobility in short and narrow devices were studied, which is most interested in future LSI applications. In comparison of hole mobilities in <110> and <100> channel directions, we should pay attention to the difference of impurity profiles at the channel caused by different halo implant directions. Hole mobility extracted by $R_{on}$, however, can be distinguished from the effect of impurity profile difference by rotating the wafer plane and transistor direction independently on the wafer (Fig. 5). Figure 6 shows $R_{on}$ curves in narrow channel SiGe pMOSFETs. For <110> channel direction, $R_{on}$ curves show the non-linearity with $L_g$, however, for <100> channel $R_{on}$ curve is almost linear with $L_g$. And there is no halo implant direction dependence between them. It is amazing and unexpected that the hole mobility is much larger in <110> direction in very short and narrow channel SiGe pMOSFETs. In addition, $R_I$ curves are insensitive to halo implant direction (Fig. 7). The non-linearity in $R_{on}$ curves can be attributed to the mobility modulation in <110> channel. The active area length and Gate-contact distance do not affect on $R_{on}$-relations (Fig. 8), therefore hole mobility degradation only depends on $L_g$ by longitudinal direction scaling. Figure 9 illustrates the schematic images of stress effects to the channel, explaining the complicated behavior above.

(4) Channel Stress Enhancement by Transistor Geometry:
To confirm the root cause of the observed phenomena, the stress simulation has been achieved for many different transistor geometries. Figure 10 shows the simulated stress magnitude in longitudinal and transverse directions with $L_g$ and $W$ scaling. Because of no major difference in hole mobilities between <110> and <100> channel in large $L_g$ and $W$ region as shown in Fig. 3, hole mobility in <110> channel should be corresponded with that in <100> channel if device geometries have same 2-dimensional biaxial stress. The solid line in Fig. 11 shows the boundary in $L_g$-$W$ plane, having the same mobilities both for <110> and <100> SiGe channels. In the side of the boundary, mobility for <110> channel is smaller than that for <100> channel. The dotted line shows the $(L_g,W)$ sets derived from stress simulation, having the same stresses both in longitudinal and transverse directions. Both lines show the excellent correspondence each other, therefore, experimentally observed mobility modulation are attributed to the stress modulation effect caused by device layout configurations. Figure 12 shows the relations of $L_g$-dependence (minimum operating gate length) where $L_g$ in <100> channel SiGe pMOSFET shows the best current drive at the same gate length.

Conclusion
The impact of transistor layout configuration on hole mobility has been systematically studied in Si and SiGe channel pMOSFETs. For the first time, it has been found that hole mobility in (100)<100> channel SiGe is the highest in short and narrow channel pMOSFETs. Therefore, recommended channel material and channel direction should be SiGe with (100)<100> for the realistic short and narrow channel pMOSFET in the future CMOS LSI towards 20 nm node and beyond.

References
Fig. 6: (a) Simulated stress distribution for SiGe channel pMOSFETs both in the longitudinal and transverse directions. (b) Simulated channel stress at the depth of 1 nm from the surface. Longitudinal and transverse compressive stresses are decreased by channel width (<110>SiGe).

Fig. 7: $V_{out}$ roll-off in narrow channel pMOSFETs with various channel directions and halo implant directions. SCE is controlled by the halo implant direction only.

Fig. 8: Impacts of Gate-Contact distance and Gate-Contact distance on $R_m$ vs $L_x$ relationships with (100)/<110> channel SiGe pMOSFETs. Both parameters are not playing a major role for $R_m$ modulation in (100) SiGe channel pMOSFETs with rotated channel directions on (100) SiGe and (100) Si. At fixed gate length, (100)/<100> channel SiGe shows the best $I_{on}$.

Fig. 9: Mobility vs. $E_p$ in (100) SiGe channel pMOSFETs with <100> and <110> directions. No major difference is observed between them.

Fig. 10: (a) Simulated stress distribution for SiGe channel pMOSFETs both in the longitudinal and transverse directions. (b) Simulated channel stress at the depth of 1 nm from the surface. Longitudinal and transverse compressive stresses are decreased by $L_x$ and $W$ scaling, respectively.

Fig. 11: Mobility and Stress phase diagram on $L_x-W$ plane for SiGe channel pMOSFETs. Solid line shows the experimentally determined ($L_x, W$) sets showing $\mu_{1100} = \mu_{1100}$. Above this line, $\mu_{1100}$ is larger than $\mu_{1100}$. Dotted line shows the simulated ($L_x, W$) relationship showing $\sigma_{yy} = \sigma_{xx}$. Excellent correspondence of both lines suggest that hole mobility should depend on stress modulation by device layout configuration.