Experimental Investigation and Modeling for Surface Roughness Limited Mobility in Strained pMOSFETs

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Abstract

This work provides an experimental assessment of surface roughness scattering limited mobility (μ_{SR}) under process-induced uniaxial strain. By accurate split C-V mobility extraction method, the μ_{SR} of advanced strained short channel devices has been extracted at cryogenic temperature to suppress phonon scattering mechanism. Our result indicates that μ_{SR} shows significant strain dependence under uniaxial stain. Furthermore, µSR has higher strain dependence than phonon scattering limited mobility (μ_{PH}) from experimental results. Finally, a wavefunction penetration model is proposed to explain the possible physical origin of the strain dependence of μ_{SR} for devices with biaxial and uniaxial stressors. The 1D quantum mechanical (QM) simulation result also supports our explanations.

Introduction

Strain technology has been considered as a key process knob beyond 90nm technology [1]. It is known that strain can reduce inter-valley phonon scattering and effective conduction mass [1]. However, whether the surface roughness limited mobility μ_{SR} can be enhanced by strain and the root cause of μ_{SR} enhancement remain controversial.

Recently, Bonno et al. [2] reported NFET µ_{SR} enhancement by biaxial tensile stress attributed to smoother surface roughness. However, the observed μ_{SR} data by Zhao et al. [3,4] showed opposite trend between NFET and PFET and cannot be easily explained by the micro-roughness of Si/SiO₂ interface.

In this work, we examine the impact of strain on μ_{SR} of pMOSFETs by process-induced uniaxial strain with He-based low temperature system and compare the strain sensitivity between μ_{PH} & $\mu_{SR}.$ In addition, the wavefunction penetration model is proposed to explain the possible physical origin of biaxial and uniaxial strain dependence of μ_{SR} . Furthermore, 1D QM simulation [14] has also been conducted to show the strain impact on wavefunction penetration levels.

Experimental Setup

pMOSFETs with channel direction <110> with neutral, tensile and compressive uniaxial Contact Etch-Stop Layer (CESL) were manufactured based on the state-of-the-art CMOS technology [6], as shown in Fig. 1. The mobility for the short channel devices was extracted by split C-V method [6]. In order to extract μ_{SR} , cryogenic temperature measurements were conducted at a probe station using liquid He as cooling source. The temperature range is from 10K to 300K. At last, we modified the 1D Sivalco simulator [14] to determine the strain impact on the carrier penetration levels [5].

Comparison of μ_{SR} & μ_{PH} Enhancement

Fig. 2 shows I_D -V_G characteristic of the devices with neutral stressor with various temperatures. Fig. 3 shows the extracted carrier mobility versus vertical electric field with various temperatures. The mobility tends to be increase as temperature decreases because phonon scattering rates are reduced. At temperature lower than 60K, the high field mobility tends to be saturated because phonon scattering mechanism is fully suppressed. Therefore, the high field mobility at temperature lower than 60K can be viewed as surface roughness limited mobility [2-4].

Fig. 4 shows the extracted carrier mobility at E_{EFF}=1.6MV/cm versus temperature with various stressors. The compressive uniaxial strain shows mobility enhancement due to band engineering and carrier repopulations [1]. μ_{SR} dominates the total mobility at temperature <60K and the temperature behaviors of all stressors are the same.

Fig. 5 shows the mobility enhancement $(\Delta \mu/\mu)$ versus temperature with various stressors. As temperature decreases, the mobility enhancement tends to be increased and saturated at temperature <60K where surface roughness scattering dominates. It indicates μ_{SR} has stronger stress sensitivity than μ_{PH} .

Wave Penetration Model & Uniaxial Strain Dependence of μ_{SR}

In order to explain the physic origin of uniaxial strain dependence on surface roughness scattering mechanism, the wavefunction penetration model proposed by Polishchuk and Hu [5] is introduced, as shown in Fig.

Department of Electronics Engineering & Institute of Electronics, National Chiao Tung University, Hsinchu, Taiwan 6. The penetration level depends on carrier attenuation length (λ) [5] and can be modeled as (1) [7]:

$$\lambda = \sqrt{\frac{\hbar^2}{2m_z \phi_b}} \tag{1}$$

with \hbar the reduced Planck's constant, m_z the out-of plane effective mass, $\Phi_{\rm b}$ the Si/SiO₂ potential barrier height. Since longer λ causes more roughness scatterings [5], the stress sensitivity of μ_{SR} ($\Delta \mu_{SR}/\mu_{SR}$) is determined by the strain engineering on m_z and Φ_b .

From the angle of the wavefunction penetration perspective, compressive uniaxial strain on <110> pMOSFETs contributes heavier outof-plane effective mass (m_z) and higher barrier height (Φ_b) [8-12], which cause shorter electron attenuation length and then lower surface roughness scattering rates. Therefore, lower surface scattering rates should be responsible for μ_{SR} enhancement in uniaxial pMOSFETs.

Wave Penetration Model for Biaxial Strain Dependence on μ_{SR}

The wavefunction penetration model may also explain previous works on biaxial strain dependence of μ_{SR} [2,3,13]. Fig. 7 shows the $\Delta \mu_{SR}/\mu_{SR}$ of NFET and PFET extracted from [2,3,13]. For NFET, Fig. 8 shows most electrons repopulate into the $\Delta 2$ valley under biaxial stress, which may result in higher $_{\rm b}$ [8-12], heavier m_z [8-12], shorter and thus larger μ_{SR} .

For PFET, the biaxial strain dependence on μ_{SR} is quite different with the uniaxial strain case. In order to explain the different behaviors, the uniaxial and biaxial strain dependence on energy band diagram and m_z of each subband are referred to [1,8]. Fig. 9 shows the PFET energy band diagram [8] and hole repopulations with uniaxial compressive stress and biaxial tensile stress, respectively. Both types of stressor result in higher _b but opposite trend for m_z. Uniaxial compressive stress increases m_z,

decreases , and consequently improves μ_{SR} . For biaxial tensile stress, is initially increased by the strain-reduced m_z, but is then decreased with increasing strain due to the strain-increased b. This explains the PFET non-monotonic behavior in Fig. 7.

Table I summarizes the polarities of stress sensitivity for m_z [8-12], Φ_{b} [8-12], λ and μ_{SR} respectively. In order to prove the strain dependence on wavefunction penetration level, a 1D QM Sivalco model [14] is modified to examine the polarities in Table I. Fig. 10 shows the electron wavefunction penetration into gate dielectric from 1D simulations. In Fig. 11, higher $_{b}$ and heavier m_{z} show lower fraction f of carrier penetration [5] from 1D QM simulations. Typically lower f means less wavefunction penetrations [5]. The result is consistent for uniaxial NFET in Table I.

Summary

By accurate split C-V mobility extraction method, the uniaxial strain dependence of μ_{SR} in advanced short channel pMOSFETs has been investigated at ultra low temperature. Our measured data indicate that μ_{SR} shows significant strain dependence under uniaxial process-induced strain. In addition, μ_{SR} has higher strain dependence than μ_{PH} . From the angle of the wavefunction penetration, compressive uniaxial strain contributes shorter electron attenuation length and thus lower surface roughness scattering rates. Furthermore, the wavefunction penetration model successfully explains the biaxial and uniaxial strain dependence of μ_{SR} . Our 1D QM simulation result also shows that the fraction f of wavefunction penetration in the gate dielectric has strong strain sensitivity and supports our explanations on the strain dependence of μ_{SR} .

Acknowledgement

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Reference

Reference [1] S. Thompson *et al.*, *IEEE TED*, p. 1010, May 2006 [2] O. Bonno *et al.*, *VLSI Symp.*, p. 134, 2007 [3] Y. Zhao *et al.*, *IEDM*, p. 577, 2008 [4] Y. Zhao *et al.*, *VLSI Symp.*, 2009 [5] I. Polishchuk and C. Hu, *VLSI Symp.*, p. 51, 2001 [6] W. P.-N. Chen *et al.*, *IEEE EDL*, p. 768, July 2008 [7] K.K. Hung *et al.*, *IEEE TED*, p. 654, Mar. 1990 [8] Y. Sun *et al.*, *JAP*, vol. 101, May 2007 [9] X. Yang *et al.*, *APL*, vol. 93, July 2008 [10] W. Zhao *et al.*, *IEEE EDL*, p. 410, 2005 [11] C. Claeys *et al.*, *SSE.*, p. 1115, 2008 [12] S. Thompson *et al.*, *IEDM*, p. 221, 2004 [13] T. Mizuno *et al.*, *IEEE TED*, p. 1114, July 2004 [14] *Atlas User's Manual*, SILVACO, Santa Clara. CA. 2008 Clara, CA, 2008

Neutral/Compressive/Tensile CESL



Fig. 1. pMOSFET schematic with neutral, tensile and compressive stressor.



Fig. 4. The extracted hole mobility at E_{EFF}=1.6MV/cm with various stressors. It shows μ_{SR} dominates the total mobility at temperature <60K.



Fig. 7. $\Delta \mu_{SR} / \mu_{SR}$ by biaxial strain extracted from the literature [2,3,13].

Stressor	Index	NFET	PFET
Biaxial-Tensile [2,3]	mz		
	Φ _b		
	λ		lower σ :
			stronger σ :
	Ξ _{SR}		lower σ :
			stronger σ :
Uniaxial-Tensile [This work]	mz		
	Φ _b		
	λ		
	Ξ _{SR}		
Uniaxial-Compressive [This work]	mz		
	Φ _b		
	λ		
	Ξ _{SR}		





Fig. 2. PFET ID-VG Characteristics with neutral stressor.



Fig. 5. The hole mobility enhancement $(\Delta \mu/\mu)$ versus temperature with various stressors. As mobility temperature decreases. the enhancement tends to be increased and is saturated at temperature <60K. It indicates μ_{SR} shows stronger stress sensitivity than μ_{PH} .



showing that most electrons repopulate into $\Delta 2$ valley under biaxial tensile stress. It may result in higher b [8-12], heavier

SiO

10

10¹

10¹

10¹

-10

Carrier Concentration (cm⁻³



Fig. 3. The extracted hole mobility versus vertical electric field with various temperatures.



Fig. 6. Electron wavefunction penetration into gate dielectric. mz is out-of plane effective mass; b is Si/SiO2 potential barrier height; is electron attenuation length. Longer causes more surface roughness scattering. [5]



Fig. 9. PFET energy band diagram and hole repopulations with uniaxial compressive stress and biaxial tensile stress.

=0.4

33

m



Fig. 10. The wavefunction penetrations into gate dielectric.

10

Fig. 11. Higher b and heavier mz show lower fraction f of carrier penetration from 1D QM simulations. It is consistent with uniaxial-Tensile NFET in Table I.

Si