

Impact of the Channel Direction Dependent Low Field Hole Mobility on Si(100)

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1. Introduction

Carrier mobility plays a critical role in the performance of MOSFETs even in the scaled down generation [1]. The low field mobility is crucial to the transport of extremely short channel transistors exhibiting the quasi-ballistic transport [2]. The strain technology is now widely used in order to reduce the effective mass of carriers to improve the mobility characteristics [3,4]. It is well known that the heavy hole effective mass has direction dependency [5]. Sayama reported the improved saturation current drivability of pMOS on (100) surface along the [001] channel direction compared to the conventional [011] direction [6]. The improvement is explained by the higher drift velocity along the [001] direction due to the smaller effective mass of heavy holes. However, the channel direction dependent low field mobility characteristic has not been experimentally confirmed yet. In this paper, we report on the measured channel direction dependent hole mobility of the pMOS fabricated on the atomically flattened (100) orientation surface where the interface roughness scattering is effectively suppressed. The impacts of the channel length, temperature and lateral electric field to the direction dependent hole mobility is clarified.

2. Experimental

pMOS devices were fabricated on the atomically flattened silicon surface and on the conventional surface. Figs. 1 (a-b) show the typical AFM images of the gate insulator film/silicon interfaces of the fabricated devices. Fig. 2 shows the measured hole mobility characteristics. A higher hole mobility has been obtained for the atomically flat device due to the suppressed interface roughness scattering [7]. Up to now, with the conventional flatness at the interface, channel direction dependent hole mobility has not been observed. For the fabricated devices, the channel direction dependency of drain current in linear region (I_{Dlin}) and mobility were carefully evaluated with transistors placed along the directions of every 15 degrees on (100) oriented silicon surface as described in Fig. 3. The process flow for the device fabrication is explained elsewhere [8].

3. Results and Discussions

Fig. 4 shows I_{Dlin} as a function of the channel direction for the devices with gate length (L_G) of 10.0 and 0.8 μm , respectively. An obvious channel direction dependency of I_{Dlin} is clearly confirmed for both of the devices at 22 K. That is, drain current takes the maximal at the [001] directions and the minimal at [011] directions, respectively. As the temperature increases, the dependency becomes smaller and vanishes out at 300 K. Fig. 5 shows the typical AFM image of the interface of the fabricated device shown in Fig. 4. The atomic step direction and step width were extracted at various spots on the fabricated 200 mm wafer, and the angles of step direction were confirmed to vary from 199~208 degree as well as the terrace width from 0.35~0.48 μm for this device, respectively. There is no clear correlation between the morphology of the atomically flat interface and the direction dependency of the obtained I_{Dlin} . On the contrary, it agrees very well with the direction dependency of the heavy hole effective mass shown in Fig. 6 [5]. Fig. 7 shows the hole mobility characteristic at 22 K

with the [001] direction and with the [011] direction for the L_G of 20 μm and 10 μm , respectively. The mobility characteristic clearly reflects the result of the channel direction dependency of I_{Dlin} shown in Fig. 4. Consequently, based on these results, it has been experimentally confirmed that the direction dependency of the heavy hole effective mass appears in the low field hole mobility characteristics. Furthermore, for $L_G=20$ μm , the increase of the hole mobility from [011] to [001] are about 8 %. However for $L_G=10$ μm , mobility along [011] direction decreases and the difference between the two channel directions are about 15 %. In any case, the mobility is higher than that of the device with the conventional interface flatness. The detailed relationship between L_G and the magnitude of the channel direction dependency of mobility is clarified as follows. Fig. 8 shows the channel conductivity extracted from the measured I_{Dlin} . Based on this result, the ratio of hole mobility along the [001] and the [011] directions was calculated, and the result is shown in Fig. 9 for various temperatures. The result shows that the ratio becomes higher for shorter L_G and reaches around 1.5 at 22K, respectively. In addition, the ratio decreases as temperature increases. Fig. 10 shows the I_{Dlin} ratio as a function of the lateral electric field measured by changing drain voltage in linear region for $L_G=10$ and 20 μm , respectively. The ratio does not change with the lateral electric field, indicating the obtained channel length dependency of the mobility characteristics is not due to the change in lateral electric field. Instead, it is explained as follows. When L_G is relatively long, holes are scattered to random directions many times. As a result, the channel direction dependency of the hole effective mass does not appear as the drain current. For shorter L_G with less carrier scattering, i.e., lower temperature and smoother interface, the carriers move towards the direction of an applied electric field and the original heavy hole effective mass to the direction impacts the drain current. This implies that the direction dependency of heavy hole effective mass will impact the low field hole mobility and drain current drivability of extremely short channel pMOS with few number of scattering events even at an operation temperature.

4. Conclusions

Under the condition that the interface roughness and phonon scatterings are suppressed for relatively short channel devices, the channel direction dependency of the hole mobility on silicon (100) surface originating from the heavy hole effective mass is clearly observed. The ratio of the low field mobility along the [001] and [011] directions increases for devices with shorter gate length and reaches around 1.5 at most. Consequently, the understanding of this hole mobility behavior is crucial for the device design optimization of pMOS in extremely short channel generation.

References

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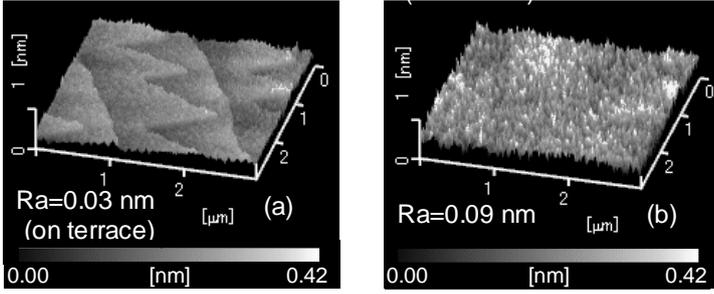


Fig. 1. AFM images at the gate insulator/silicon interface of the fabricated MOSFETs on (a) atomically flat surface, and (b) conventional surface, respectively.

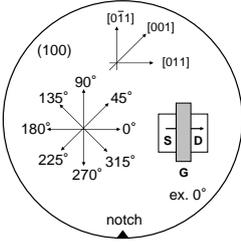


Fig. 3. schematic illustration of the pMOS with various channel directions on the fabricated (100) wafer.

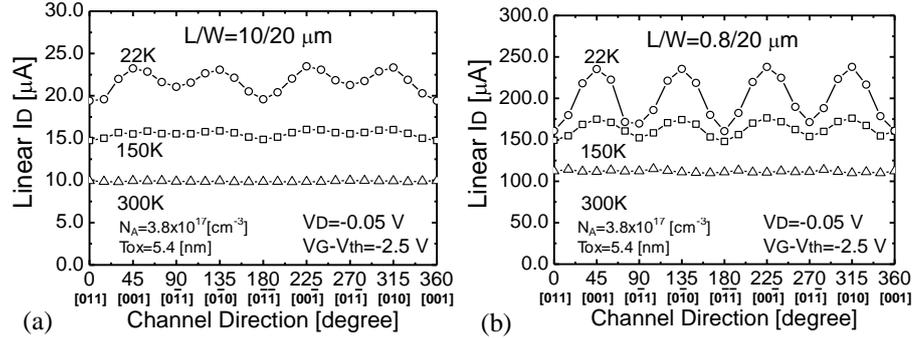


Fig. 4. Linear drain current (I_{Dlin}) as a function of channel direction angle measured at various temperature. (a) $L/W = 10/20 \mu\text{m}$, and (b) $0.8/20 \mu\text{m}$, respectively. I_{Dlin} clearly depends on the channel angle at 22 K for both gate sizes. A stronger dependence is observed for pMOS with shorter channel length.

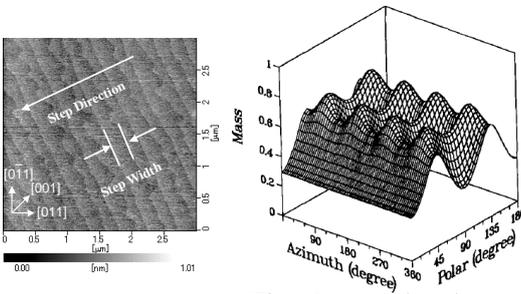


Fig. 5. Typical AFM image of the fabricated device's interface.

Fig. 6. Angular dependence of the hole directional mass at 1meV above the band edge [5].

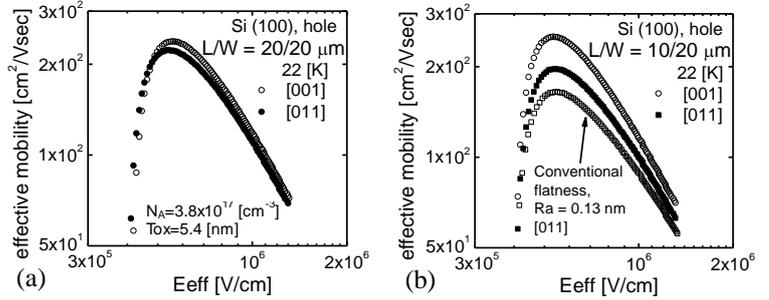


Fig. 7. μ_{eff} v.s. E_{eff} at 22 K for (a) $L/W=20/20 \mu\text{m}$ and (b) $10/20 \mu\text{m}$, respectively. Channel direction dependence of the hole mobility is obtained for both cases. The difference of the mobility is larger for the device with shorter gate length.

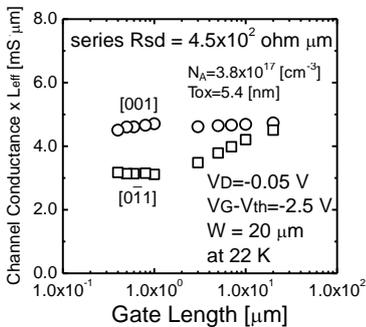


Fig. 8. Extracted channel conductivity as a function of gate length. The Conductivity maintains at a constant with [001] direction while decreases as channel length decreases with [011] direction, respectively.

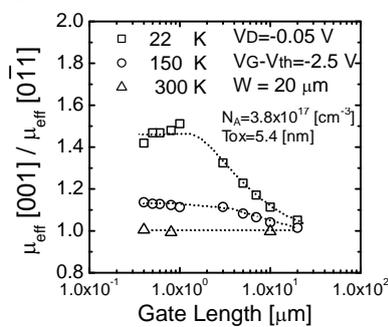


Fig. 9. Ratio of effective hole mobility along the [001] and [011] directions as a function of gate length at various temperatures. Mobility ratio is about 1.5 at most.

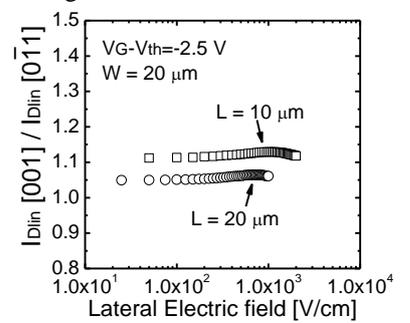


Fig. 10. Ratio of I_{Dlin} as a function of lateral electric field in the channel for gate length of 10 and 20 μm , respectively. The current ratio does not depend on the lateral electric field in the linear region.

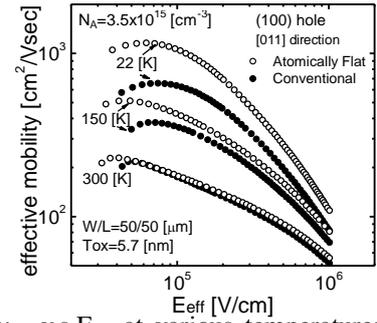


Fig. 2. μ_{eff} v.s. E_{eff} at various temperatures for pMOS on atomically flat and conventional surfaces, respectively.