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Tunnel FET Promise and Challenges

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Abstract

This paper reviews recent advancements in tunnel field effect transistor (TFET) technology and assesses its promise for overcoming the energy efficiency limit of CMOS technology. Challenges for practical implementation of low-cost, low-power TFET digital logic are discussed.

Introduction

Increasing power density has become a major challenge for continued MOSFET scaling, due to non-scalability of the sub-threshold swing (S) which limits reductions in threshold voltage (V_T) and power supply voltage (V_{DD}) [1]. Alternative transistor designs that offer steeper switching behavior than a MOSFET, *i.e.* which can achieve the required on/off current ratio (I_{ON}/I_{OFF}) at a lower V_{DD}, are needed to surmount this challenge. Band-to-band tunneling (BTBT) current can be modulated more abruptly than thermionic emission current; therefore a TFET (Fig. 1) can in principle achieve S < 60 mV/dec [2] hence higher I_{ON}/I_{OFF} at low V_{DD}. Depending on the performance requirements, then, TFETs can allow for lower voltage operation to mitigate the CMOS power crisis.

This paper reviews recent advancements to improve the performance of TFETs and discusses remaining challenges for their practical use in low-power digital circuits.

$Si_{1-x}Ge_x$/Si TFETs

Since BTBT current increases exponentially with decreasing band-gap energy (E_G), the use of $Si_{1-x}Ge_x$ or Ge as the tunneling material has been proposed to improve TFET I_{ON} [3,4,5]. Demonstrated $Si_{1-x}Ge_x$ and Ge TFETs have undesirably higher I_{OFF}, however. A heterojunction design, in which the $Si_{1-x}Ge_x$ or Ge is used only in the source region (while Si is used in the channel and drain regions), can maintain low I_{OFF} [5,6]. TFETs with Ge as the source material (Fig. 2) have been demonstrated to achieve the highest I_{ON}/I_{OFF} for low-voltage (0.5 V) operation thus far [7]. Fig. 3 compares the projected energy-delay performances of Ge-source TFET technology [7] *vs*. CMOS technology [8] at 22 nm gate length (L_G). The steeper switching behavior of the Ge-source TFET potentially can provide for lower delay at voltages below ~0.4V hence lower energy per operation at sub-500MHz frequencies. The use of a high-permittivity gate dielectric material and a gate-all-around (GAA) structure provides for superior gate control and hence better projected performance [9].

Advanced TFET Materials

The range of performance over which TFETs offer an advantage over MOSFETs can be extended if more advanced semiconductor materials are used. III-V and carbon materials are of particular interest due to their small tunneling effective masses and direct band gaps. The most promising III-V materials for TFETs appear to be InAs (n-channel) [10] and $InAs/Al_xGa_{1-x}Sb$ (p-channel) [11]. Fig. 4 compares various simulated TFET transfer characteristics. Carbon nanotube (CNT) [12] and graphene nanoribbon (GNR) [13] TFETs potentially can achieve even lower average S because the tunneling probability is higher in a 1D system than in 2D and 3D systems due to the lack of transverse momentum, and also because the 1D density-of-states distribution can provide for high carrier density at small Fermi energy, allowing large tunneling current to be achieved with a small voltage swing [14].

TFET Technology Challenges

The ability to tune V_T is an important requirement for circuit design optimization. To date, no systematic study of TFET V_T control has been reported. Process-induced V_T variation can limit V_{DD} scaling and should be studied.

Because a TFET comprises a reverse-biased pn junction, channel-length (*i.e.* off-state depletion width) scaling below ~20 nm will result in significantly increased I_{OFF} [15]. This issue can be mitigated by elevating the source region (Fig. 5) to allow for more aggressive L_G scaling [16].

Since a TFET is an asymmetric structure, it cannot be used effectively in a transmission/pass gate or as an access transistor because these applications require current flow in both directions. This limits the utility of TFETs in static latches/registers and conventional 6-transistor SRAM cells. For a TFET-based SRAM cell to achieve good read and write margins, an additional read access transistor is needed – at the cost of increased cell area [17]. The series connection of TFETs (*vs.* MOSFETs) in standard pull-down/pull-up networks will also require more area.

Because the channel-region inversion layer in a TFET is linked to the drain (rather than the source as in a MOSFET), larger gate-to-drain ("Miller") capacitance is another concern for TFET-based circuit design [18]. For lightly loaded gates ($C_{out}/C_{in} < 4$), this increased capacitive loading can significantly degrade circuit performance [17,18].

Conclusion

TFETs show promise for improving CMOS energy efficiency. To extend the potential advantage of TFET technology beyond low-throughput/high-parallelism applications, substantial improvements in I_{ON} via innovation in device design and advanced materials are needed.

Fundamental challenges pertaining to V_T control, L_G scaling, and TFET-based circuit design remain to be addressed before TFET technology can be considered to be practical for the manufacture of low-power digital circuits.

References

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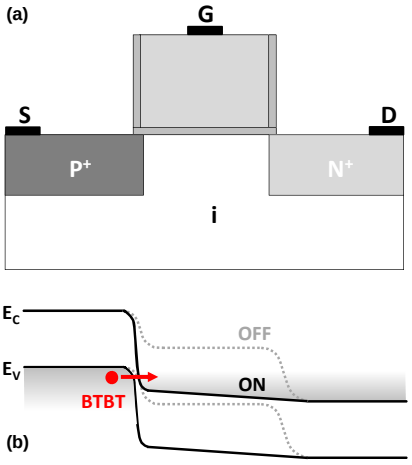

Fig. 1: (a) Schematic cross-section of a basic TFET structure. (b) Energy band diagram showing the device operating principle.

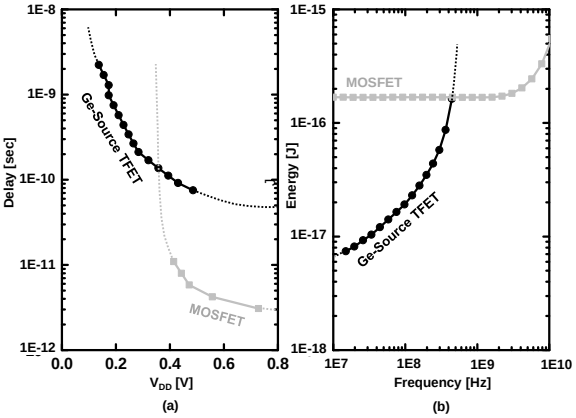

Fig. 3: Comparison of 30-stage FO1 inverter chain performance for planar Ge-source TFET [7] *vs*. MOSFET [8] technologies at 22 nm L_G. (a) minimum-energy delay *vs*. V_{DD} (b) energy/cycle *vs*. frequency.

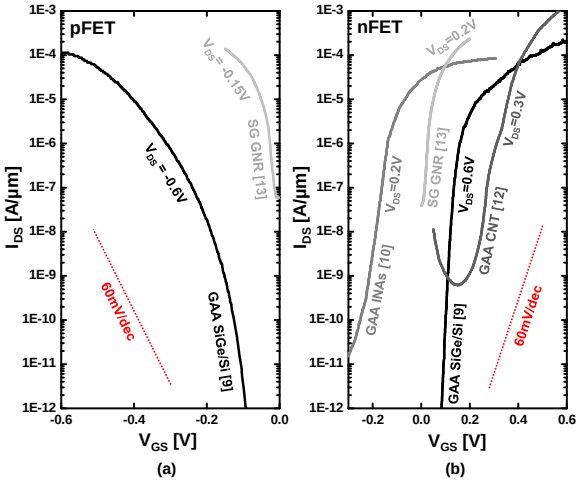

Fig. 4: Simulated TFET transfer characteristics for (a) p-channel and (b) n-channel devices.

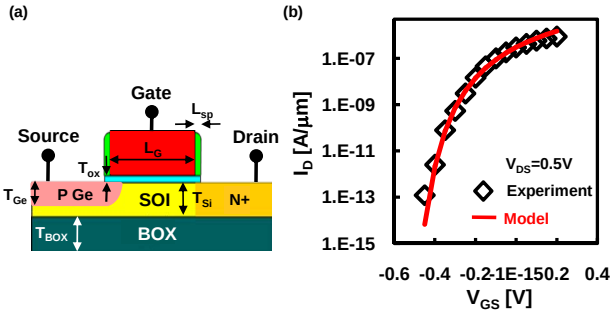

Fig. 2: (a) Schematic cross-section of a planar Ge-source TFET. (b) Measured Ge-source TFET I-V characteristics (L_G = 5um, T_{OX} = 3nm, T_{BOX} = 200nm, T_{Si} = 70nm, T_{Ge} = 21nm, and L_{SP} = 8nm).

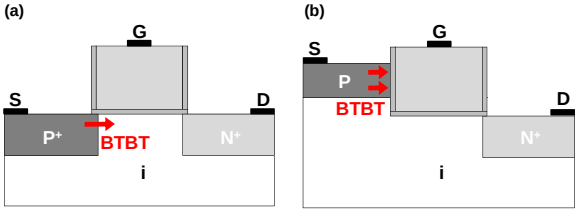

Fig. 5: Comparison of (a) planar *vs*. (b) elevated source TFET structures.