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Optimization of Silicon p-channel Tunnel FET with Dual κ Spacer

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1. Introduction

Tunnel FET (TFET) with it's sub 60 mV/decade, is emerging as an attractive candidate for low power applications. However the TFETs have poor ON current. The performance of p-channel TFET (pTFET) has been improved by reducing the tunneling barrier height using low band gap material [1, 2] and also by reducing the tunneling barrier width using high κ gate dielectric [3]. The use of these techniques increases both ON current (I_{ON}) and OFF current (I_{OFF}). Hetero junctions architectures have been used in our previous work to improve I_{ON} of pTFET [4].

In this paper we have explored the use of dual κ spacer with pTFET to improve I_{ON} with negligible effect on I_{OFF}. A dual-κ spacer concept is proposed and evaluated in underlap and non underlap silicon pTFETs for the first time using extensive device simulations. The dual-κ spacer consist of an inner layer made of a high-κ (hk) material and an outer layer made of a low-κ (lk) material (Fig. 1).

2. Device Structure and Simulation Setup

Fig. 1 shows the structures of silicon pTFET with dual-κ spacer. Gaussian doping profiles with gradients of 2 nm/dec are used. The hk spacer width is 2 nm except for the spacer width study. 2-D device simulations were performed using Synopsys TCAD tool SENTAURUS [5]. The nonlocal tunneling model with the band edge tunneling masses of m_c = 0.65m_0 and m_v = 0.65m_0 (where m_0 is the electron rest mass) for silicon are used. Fig. 2 shows the excellent fit of this nonlocal tunneling model with the experimental data from Fair and Wivell [6] for a reverse biased Si Zener diode.

3. Optimization of pTFET

Effect of Dual κ Spacer on Non Underlap Structure

The use of dual κ spacer with non underlap structure (Fig. 1(i)) increases the tunneling current compared to pTFET with oxide spacers (Fig. 1(i) with hk=lk=3.9) as seen in Fig. 3. This is due to increase in the gate fringe field coupling to the source-channel junction (Fig. 4). This reduces the tunneling width as seen from the band diagram of Fig. 5, thereby improving the tunneling current.

Effect of Dual κ Spacer on Underlap Structure

The fringe field lines can be made denser near the source-channel junction (Fig. 4) by shifting the hk spacer towards the channel resulting into a 2 nm gate-source/drain underlap (Fig. 1(ii)). This further reduces the tunneling width (Fig. 5) and improves the tunneling current along with subthreshold slope (SS) as seen in Fig. 3.

Effect of the Underlap Length

For the underlap structure, the width of hk spacer is varied by moving the edge closer to the gate while keeping the edge common with the low κ spacer fixed. Hence the underlap created is equal to the hk spacer width.

For underlap length (same as hk spacer width) of 0, the fringe field is spread through the lk dielectric (SiO_2). As the hk spacer is introduced, there is a significant concentration of the fringe field near the junction. Hence the I_{ON} increases as the underlap length increases upto an underlap length of 2 nm (Fig. 6). As the hk spacer thickness (and hence the underlap length) is further increased, the fringe field coupling through it gets spread, thereby reducing the electric field at the source-channel junction. This results in an optimum value of 2 nm for the underlap length.

Effect of the Spacer Dielectric Constant

As the κ of the hk spacer is increased from 3.9 to 45 for the underlap structure, the near end fringe field coupling closer to the gate dielectric increases, I_{ON} increases consistently and the average SS is found to decrease consistently (Fig. 7). As the κ of the lk spacer is increased from 1 to 10, the far end fringe field coupling closer to the top of the gate electrode decreases, the I_{ON} decrease consistently and the average SS increase consistently (Fig. 8). The optimal performance is for lk=1 which represents the case of air spacer and the maximum hk value that can be fabricated.

4. Conclusions

The fringe fields through spacer can be engineered to improve the performance of tunnel FETs. It is shown that the fringe fields coupling to the source - channel junction can be improved by using a dual-κ spacer with a high-κ inner layer and a low-κ outer layer, and by using a underlap structure. I_{ON} improves as the inner spacer κ is increased and the outer spacer κ is reduced. The thicknesses and the dielectric constants of the spacer layers can be optimized to obtain optimum performance.

Acknowledgment

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References

[1] F. Mayer et al. Tech. Dig. IEDM (2008) 163.
[2] C. Royer et al. Tech. Dig. ULIS (2009) 53.
[3] K. Boucart et al. IEEE Trans. Elec. Dev. vol. **54** (2007) 1725.
[4] H. G. Virani et al. Jpn. J. Appl. Phys. vol. **49** (2010) 04DC12.
[5] Synopsys TCAD Design Suite. http://www.synopsys.com
[6] R. B. Fair et al. IEEE Tran. Elec. Dev. vol. **23** (1976) 512.
[7] S. Mookerjea et al. IEEE Elec. Dev. Lett. vol. **30** (2009) 1102.

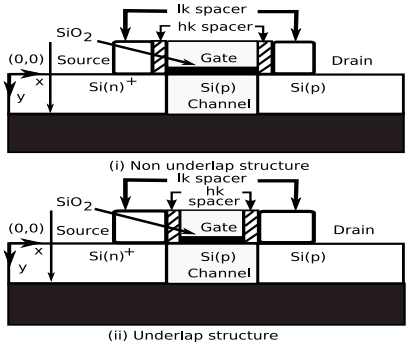

Fig. 1. The pTFET structures with dual-κ spacer: (i) Non underlap structure (L_g=20nm). (ii) Underlap structure (L_g=16nm). Gate dielectric is 1.1nm oxide, workfunction is 5.2 eV and SOI thickness is 20nm.

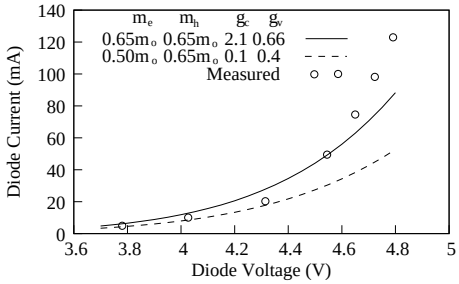

Fig. 2. The simulated Si Zener diode characteristic fitted to experimental data from Fair and Wivell [6]. The characteristic generated with the reported data in literature is also shown with dashed line [7].

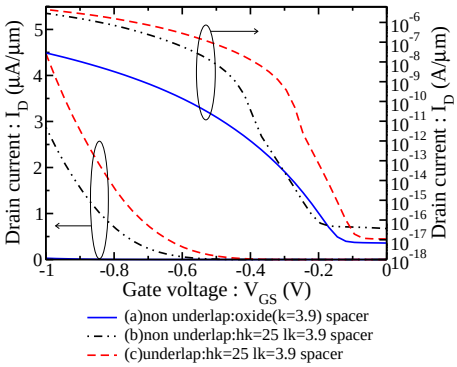

Fig. 3. $I_D V_{GS}$ characteristic for (a) non underlap pTFET structure with SiO_2 spacer, (b) non underlap pTFET structure with dual-κ spacer made of HfO_2 and SiO_2 and (c) underlap pTFET structure with dual-κ spacer made of HfO_2 and SiO_2.

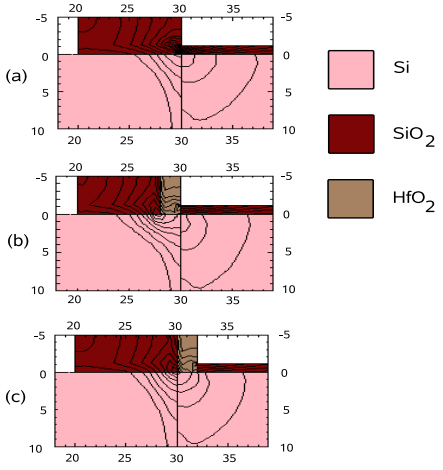

Fig. 4. Fringe field coupling through spacer for the three cases shown in Fig. 3. Dimensions are in nanometers. V_{DS}= V_{GS} = 1V.

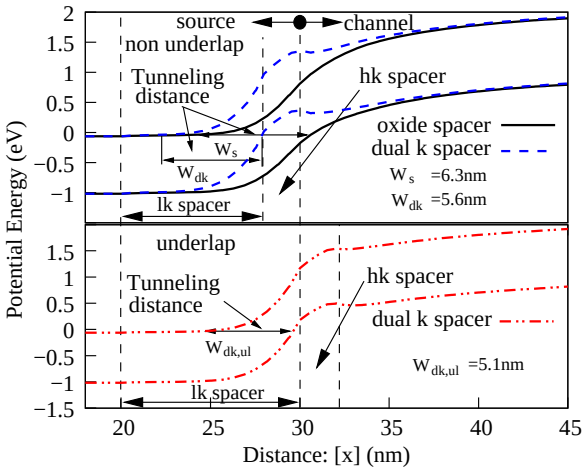

Fig. 5. Band diagram for pTFET with (a) SiO_2 spacer and dual-κ spacer in non underlap structure and (b) dual-κ spacer in underlap structure. V_{DS} = V_{GS} = 1V.

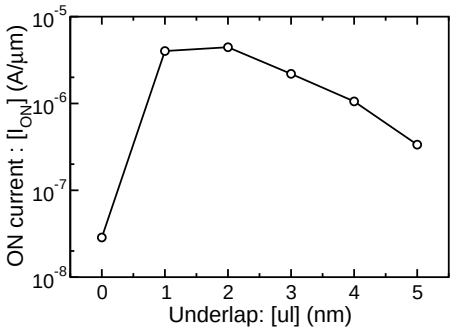

Fig. 6. Effect of hk spacer (κ = 25) width (underlap length) variation on I_{ON} of the underlap pTFET. The lk spacer (κ = 3.9) width is 10nm.

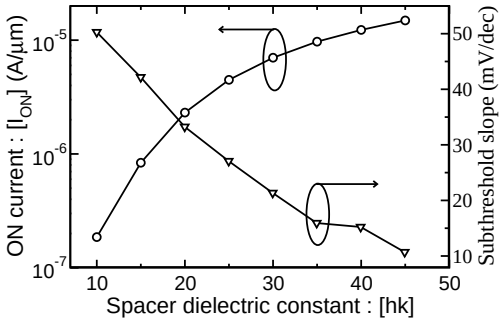

Fig. 7. Effect of the κ of the hk spacer (2 nm width) on DC characteristics of the underlap pTFET with SiO_2 (κ = 3.9) lk spacer of width 10nm.

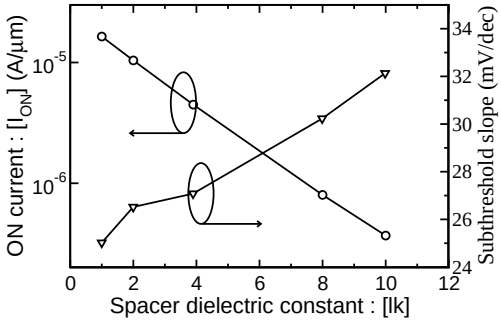

Fig. 8. Effect of the κ of the lk spacer (10nm width) on DC characteristics of underlap pTFET with HfO_2 (κ = 25) hk spacer of width 2 nm.