Metal Schottky S/D Technology of Ultra Thin SOTB (Silicon on Thin Box) MOSFET

Aki Shima, Nobuyuki Sugii, Nobuyuki Mise, Digh Hisamoto, Ken-ichi Takeda, and Kazuyoshi Torii
Central Research Laboratory, Hitachi, Ltd., 1-280, Higashi-koigakubo, Kokubunji, Tokyo 185-8601, Japan
Phone: +81-42-323-1111(ext. 3315), Fax: +81-42-327-7768, e-mail: akio.shima.yw@hitachi.com

Abstract
This paper reports novel, non-epitaxial raised Source/Drain (S/D) approaches to decrease the parasitic external resistance in MOSFET fabricated on Ultra-thin silicon on insulator (UT-SOI) utilizing metal Schottky S/D process for low stand-by power (LSTP) application of CMOS. Selectively deposited NiSi$_2$ with dopant segregation fabricated by laser spike annealing (LSA) significantly lowered effective Schottky-barrier height, and hence the contact resistance (pc). External parasitic resistance was reduced to 140 (NMOS)/350 (PMOS) Ω-μm to satisfy the needs of UT-SOI MOSFET in 32 nm node. We have shown that the component of pc in parasitic resistance is important to improve the device performance of UT-SOI MOSFET.

Introduction
Ultra-thin silicon on insulator (UT-SOI) CMOS transistors have the advantage of improved short channel effect (SCE), reduced parasitic junction capacitance and minimal floating body. In addition, ultra-thin BOX (UT-SOBI) with UT-SOI (silicon on thin BOX-SOTB) technology is getting much interests because of its possibility to reduce Vth variations and power consumption [1-3]. A key challenge in fabricating high performance UT-SOI devices is the external parasitic source drain resistance (Rsd). Typically an epitaxial-Si raised Source/Drain (S/D) is implemented to address this issue, but this process adds significant device integration complexity such as to minimize implant-related damages for the single-crystallinity of epi-Si and to control the facet of raised Si for minimized gate-to-S/D parasitic capacitance [4]. Schottky-barrier (SB)-MOSFETs are also receiving increased attention owing to their advantage of superior scalability, low extrinsic parasitics. However, they still show a substantially lower intrinsic on- and off-state performance owing to the existence of the SB. Recently, it has been demonstrated that dopant segregation (DS) is an effective means to improve the device characteristics of SB-MOSFETs [5,6]. In this paper, we report for the first time, Ultra Thin Silicon on Thin Box (UT-SOTB) MOSFETs using an alternative non-epitaxial raised S/D approach utilizing DS technique for decreasing the parasitic external resistance. The impact of DS on the electrical behavior of SB-MOSFETs is also shown.

Experimental
Figure 1 and 2 summarize the process flow and feature of the fabricated device with DS using nickel silicidation. DS was achieved by Ion Implantation (I.I.) prior to silicidation process. This process laterally segregates dopants at the interface of SOI layer. Figure 11 shows Ion and I_off plots for the SOTB MOSFETs as functions of back-gate bias (Vbs). By applying a forward bias in DS-MOSFET, Ion can be increased and that in NiSi$_2$ DS-MOSFET is strongly dependent on Vbs. This result suggests that UT-SOTB MOSFETs with DS closer to the channel is quite effective to control Ion with reduced power consumption by Vbs. In Fig. 12, energy band diagrams for Schottky UT-SOTB MOSFET are illustrated to show this effect of Vbs. Narrower depletion layer at the Schottky interface increases field emission current (I_{FE}) and effectively decreases SBH.

Conclusions
We succeeded to develop an alternate approach to decreasing external parasitic resistance in UT-SOTB MOSFET selective Schottky metal S/D process without the complexity of an epitaxial-Si raised S/D process. It was confirmed that the component of contact resistance in parasitic external resistance is significantly important to improve the device performance of UT-SOTB MOSFET. This approach is fully compatible with a conventional CMOS process flow and eliminates the added complexity of a conventional raised S/D approach.

References
Fig. 1 Process flow of Schottky UT-SOTB MOSFET with DS during NiSi formation.

Fig. 2 Schematic cross section of Schottky UT-SOTB MOSFET fabricated as shown in Fig. 1.

Fig. 3 TEM image of Schottky UT-SOTB MOSFET with NiSi2 Schottky S/D and NiSi2 FUSI gate.

Fig. 4 Dependence of XRD spectra on annealing conditions for Ni silicidation.

Fig. 5 Arrhenius plot of junction leakages in NiSi2/Si Schottky diodes and extracted SBH values.

Fig. 6 (a) Sub-threshold Id-Vg (b) Id-Vd characteristics of CMOS devices with NiSi2 Schottky S/D and NiSi2 FUSI gate: Lg = 50 nm.

Fig. 7 Dependence of Lμ-Lαf characteristics on the laser power of LSA Vd @ ±1.2V.

Fig. 8 Vth roll-off characteristics of Schottky UT-SOTB MOSFET with dopant segregation during NiSi2 formation.

Fig. 9 Comparison of Lμ-Lαf characteristics in UT-SOTB MOSFETs Vd @ ±1.2V: Results of DS-MOSFETs with Selective-W and NiSi2 are compared to that of Si Epi-MOSFET.

Fig. 10 Comparison of Ron in UT-SOTB MOSFETs: Ron of DS-MOSFETs with NiSi2 is improved compared to that of Si Epi-MOSFET.

Fig. 11 Ion and Ioff plots of UT-SOTB MOSFETs as functions of Vbs: Ion of DS-MOSFET with NiSi2 most strongly increases with Vbs.

Fig. 12 Energy band diagrams for Schottky UT-SOTB MOSFET to show the effect of Vbs: Narrower depletion layer at the Schottky interface increases field emission current (Ion) and effectively decreases SBH.