Extended Abstracts of the 2010 International Conference on Solid State Devices and Materials, Tokyo, 2010, pp695-696

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Metal Schottky S/D Technology of Ultra Thin SOTB (Silicon on Thin Box) MOSFET

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Abstract

This paper reports novel, non-epitaxial raised Source/Drain (S/D) approaches to decrease the parasitic external resistance in MOSFET fabricated on Ultra-thin silicon on insulator (UT-SOI) utilizing metal Schottky S/D process for low stand-by power (LSTP) application of CMOS. Selectively deposited $NiSi_2$ with dopant segregation fabricated by laser spike annealing (LSA) significantly lowered effective Shottky-barrier height, and hence the contact resistance (ρc). External parasitic resistance was reduced to 140 (NMOS)/ 350 (PMOS) Ω-μm to satisfy the needs of UT-SOI MOSFET in 32 nm node. We have shown that the component of ρc in parasitic resistance is important to improve the device performance of UT-SOI MOSFET.

Introduction

Ultra-thin silicon on insulator (UT-SOI) CMOS transistors have the advantage of improved short channel effect (SCE), reduced parasitic junction capacitance and minimal floating body. In addition, ultra-thin buried oxide (BOX) with UT-SOI (silicon on thin BOX:SOTB) technology is getting much interests because of its possibility to reduce Vth variations and power consumption [1-3]. A key challenge in fabricating high performance UT-SOI devices is the external parasitic source drain resistance (Rsd). Typically an epitaxial-Si raised Source/Drain (S/D) is implemented to address this issue, but this process adds significant device integration complexity such as to minimize implant-related damages for the single-crystallinity of epi-Si and to control the facet of raised Si for minimized gate-to-S/D parasitic capacitance [4]. Schottky-barrier (SB)-MOSFETs are also receiving increased attention owing to their advantage of superior scalability, low extrinsic parasitics. However, they still show a substantially lower intrinsic on- and off-state performance owing to the existence of the SB. Recently, it has been demonstrated that dopant segregation (DS) is an effective means to improve the device characteristics of SB-MOSFETs [5,6]. In this paper, we report for the first time, Ultra Thin Silicon on Thin Box (UT-SOTB) MOSFETs using an alternative non-epitaxial raised S/D approach utilizing DS technique for decreasing the parasitic external resistance. The impact of DS on the electrical behavior of SB-MOSFETs is also shown.

Experimental

Figure 1 and 2 summarize the process flow and feature of the fabricated device with DS using nickel silicidation. DS was achieved by Ion Implantation (I.I.) prior to silicidation process. This process laterally segregates dopants at the interface of SOI channel and nickel silicide. To completely convert the Si layer in S/D region into silicide with suitable lateral and without excess silicidation in thin and short Si-channel of UT-SOTB MOSFETs, nickel disilicide ($NiSi_2$) was formed by laser spike annealing (LSA) [7].

Device Characteristics

A cross sectional TEM image is shown in Fig. 3. Annealing with ultra-short duration and high temperature by LSA enables the transition to epitaxial-$NiSi_2$ with less agglomerations and less interfacial facets. As a result, selectively raised S/D structure of 30 nm- $NiSi_2$ with cubic crystalline structure was formed by vertical reaction. XRD observation revealed that reaction products transform to $NiSi_2$ after LSA+Low temperature rapid thermal annealing (RTA). Schottky-barrier height (SBH, ϕB) was extracted from the I-V characteristics of the fabricated Schottky diodes [8]. The slope of activation energy can be used to evaluate the effective SBH that includes barrier lowering effects and contributions due to thermo-ionic field emission. Our measurements clearly show that our process leads to the effective SBH lowering (Fig. 5). Ideal Id-Vg characteristics are obtained with a sub-threshold swing close to the theoretical limit (60 mV / decade at room temperature) for 50 nm-Lg MOSFET (Fig. 6(a)). A significantly improved off-state with almost ideal inverse sub-threshold slope was indicative of a strongly reduced SBH. The MOSFETs with doped $NiSi_2$ S/D show improved Ids compared to those without SBH I.I., caused by the small SBH and hence the small contact resistance (ρc) between the $NiSi_2$ S/D and Si channel due to the dopant segregation. We also observed that Ids increased with laser power of LSA, this is obviously the consequence of higher activation of segregated dopant by LSA. These results indicate that the amounts of segregated dopants modulate the SBH, thus the carrier injection at the source is enhanced. Upward sloping at low gate voltage (Vg) has been observed for short-channel SB -MOSFETs and can be invoked as the characteristic signature of a reverse-biased Schottky junction. SCE remains negligible despite high concentration of DS layer near the channel and remains well controlled at Lg down to 40 nm (Fig. 8). Vth for low stand-by power (LSTP) applications is achieved with the fully di-silicide (FUSI) $NiSi_2$ gate, which causes only slight Vth shifts due to the difference of work function between the NiSi and $NiSi_2$ FUSI metal.

The I_{on} improvement can be seen in comparison between DS- and Si Epi-UT-SOTB MOSFET [1, 3](Fig. 9). Figure 10 also compares S/D series resistance (Ron) and the Ron of DS-MOSFET is improved compared to Si Epi-MOSFET. Reduction of SBH and ρc due to DS significantly contributes to these performance improvements, since raised S/D height in Si Epi-MOSFET (60 nm) is thicker than the ones in DS-MOSFET (30 nm-$NiSi_2$) and a component of parasitic resistance: S/D diffusion resistance in DS-MOSFET is quite larger due to the ultra-thin SOI layer. Figure 11 shows I_{on} and I_{off} plots for the SOTB MOSFETs as functions of back-gate bias (Vbs). By applying a forward bias in DS-MOSFET, I_{on} can be increased and that in $NiSi_2$ DS-MOSFET is strongly dependent on Vbs. This result suggests that UT-SOTB MOSFETs with DS closer to the channel is quite effective to control I_{on} with reduced power consumption by Vbs. In Fig. 12, energy band diagrams for Schottky UT-SOTB MOSFET are illustrated to show this effect of Vbs. Narrower depletion layer at the Schottky interface increases field emission current (I_{FE}) and effectively decreases SBH.

Conclusions

We succeeded to develop an alternate approach to decreasing external parasitic resistance in UT-SOTB MOSFET selective Schottky metal S/D process without the complexity of an epitaxial-Si raised S/D process. It was confirmed that the component of contact resistance in parasitic external resistance is significantly important to improve the device performance of UT-SOTB MOSFET. This approach is fully compatible with a conventional CMOS process flow and eliminates the added complexity of a conventional raised S/D approach.

References

[1] Y. Morita, et.al., 2008 Symp. VLSI Tech., p166, [2] S. Monfray, et.al., IEDM 2007, p693, [3] R. Tsuchiya, et.al., IEDM 2007, p475, [4] K.Cheng, et.al., 2009 Symp. VLSI Tech., p212, [5] A. Kinoshita, et.al.,2005 Symp. VLSI Tech, p158, [6] C.H. Ko, et.al., 2006 Symp. VLSI Tech., p98, [7] A. Shima, et.al., 2004 Symp. VLSI Tech., p174, [8] E. Dubois, et.al., J. Appl. Phys., vol. 96, no. 1, pp. 729(2004), [9]R.T. Tung et. al. Phys. Rev. Lett. 66, pp. 72 (1991)

- Thin-BOX SOI (SOI 25nm, BOX 10nm)
- Shallow Trench Isolation
- Well Ion Implantation (I.I.)
- Gate Oxynitride Formation
- Poly Gate Patterning
- 1st Spacer Formation
- S/D I.I.
- RTA
- Spacer Removal
- *SBH (Dopant Segregation) I.I.*
- 2nd Thin Spacer Formation
- *$NiSi_2$ S/D&FUSI Gate formation (LSA+Low Temp. RTA)*
- Metallization

Fig. 1 Process flow of Schottky UT-SOTB MOSFET with DS during $NiSi_2$ formation

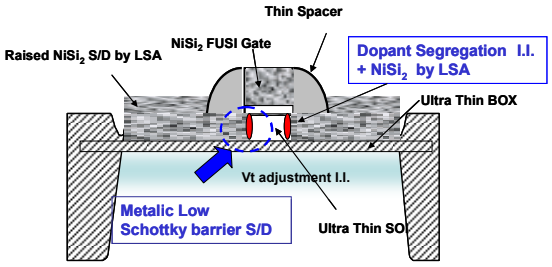


Fig. 2 Schematic cross section of Schottky UT-SOTB MOSFET fabricated as shown in Fig. 1

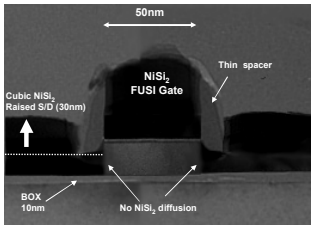


Fig. 3 TEM image of Schottky UT-SOTB MOSFET with $NiSi_2$ Schottky S/D and $NiSi_2$ FUSI gate

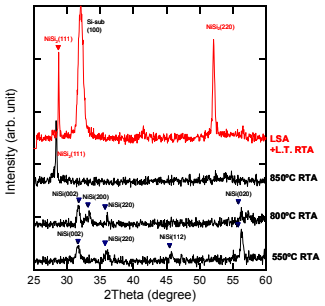
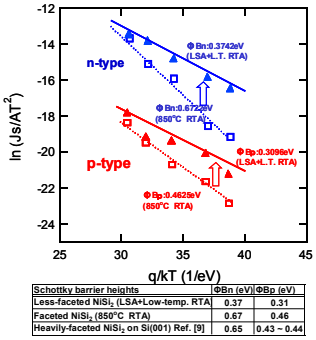


Fig. 4 Dependence of XRD spectra on annealing conditions for Ni silicidation



Schottky barrier heights	ΦBn (eV)	ΦBp (eV)
Less-faceted $NiSi_2$ (LSA+Low-temp. RTA	0.37	0.31
Faceted $NiSi_2$ (850°C RTA)	0.67	0.46
Heavily-faceted $NiSi_2$ on Si(001) Ref. [9]	0.65	0.43 ~ 0.44

Fig. 5 Arrhenius plot of junction leakages in $NiSi_2$/Si Schottky diodes and extracted SBH values

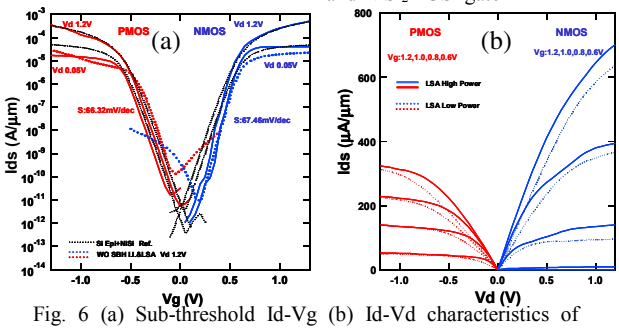


Fig. 6 (a) Sub-threshold Id-Vg (b) Id-Vd characteristics of CMOS devices with $NiSi_2$ Schottky S/D and $NiSi_2$ FUSI gate : Lg = 50 nm

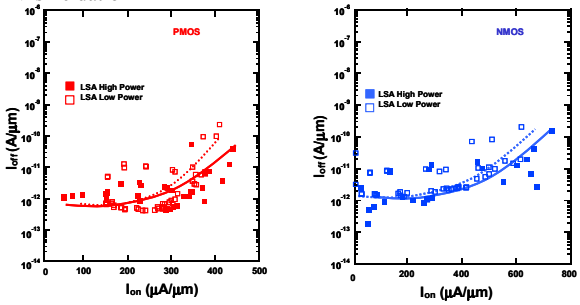


Fig. 7 Dependence of I_{on}-I_{off} characteristics on the laser power of LSA :Vd @ ±1.2V

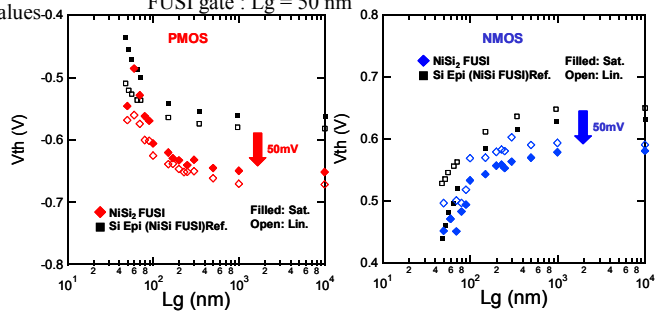


Fig. 8 Vth roll-off characteristics of Schottky UT-SOTB MOSFET with dopant segregation during $NiSi_2$ formation

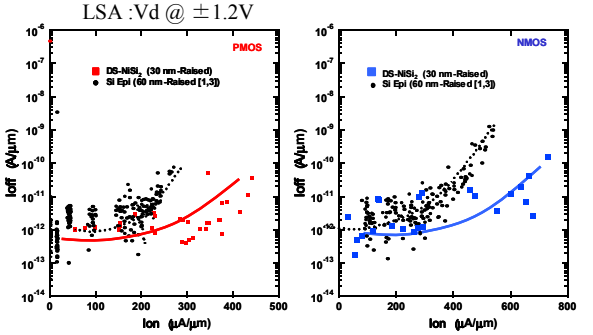


Fig. 9 Comparison of I_{on}-I_{off} characteristics in UT-SOTB MOSFETs Vd @ ±1.2V: Results of DS- MOSFETs with selective-W and $NiSi_2$ are compared to that of Si Epi-MOSFET.

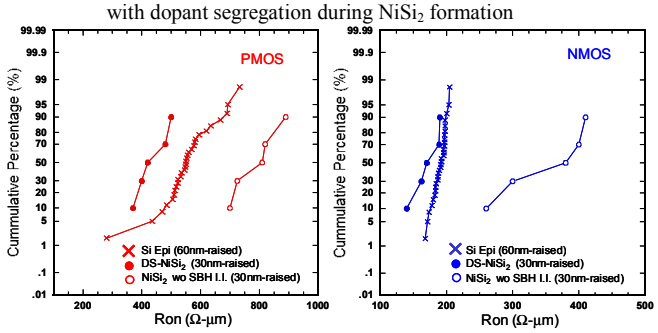


Fig. 10 Comparison of R_{on} in UT-SOTB MOSFETs: R_{on} of DS- MOSFETs with $NiSi_2$ is improved compared to that of Si Epi-MOSFET.

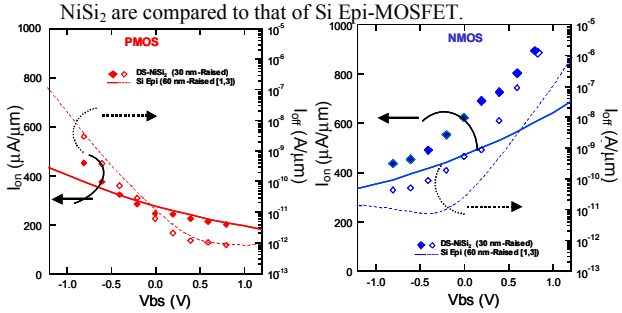


Fig. 11 I_{on} and I_{off} plots of UT-SOTB MOSFETs as functions of Vbs: I_{on} of DS- MOSFET with $NiSi_2$ most strongly increases with Vbs.

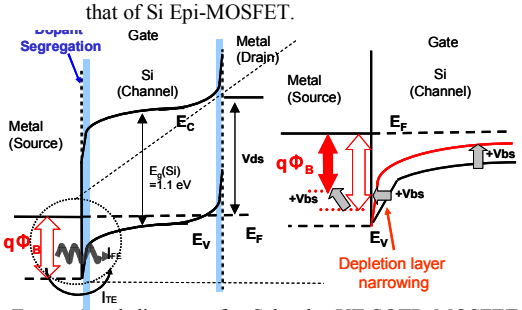


Fig. 12 Energy band diagrams for Schottky UT-SOTB MOSFET to show the effect of Vbs: Narrower depletion layer at the Schottky interface increases field emission current (I_{FE}) and effectively decreases SBH.