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Device Engineering to Improve SRAM Static Noise Margin

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1. Introduction

As the supply voltage scales down, reliability has become a major issue for the design of static random access memory (SRAM). Static noise margin (SNM) is a widely adopted metric for SRAM stability [1]. However, beyond the 22nm technology node, circuit-level techniques alone may be insufficient to ensure stability. Device engineering that specifically targets SRAM application is necessary and effective for improving the SRAM SNM. In this paper, we examine the impact of device I-V characteristics on SRAM SNM by analyzing the switching trajectories. Based on our analysis, we make suggestions for device engineering to improve the SRAM stability for future technology. 12.3% and 12.4% improvement in the read and write static noise margins are achieved by decreasing the drain-induced barrier lowering (DIBL) of the pull down and the access transistor from 150mV/V to 50mV/V.

2. Device Model and Simulation Methodology

A fast IV behavioral model containing essential physics [2] is used to include the critical features of MOSFETs, such as mobility enhancement and threshold voltage roll-off. Parameters are calibrated to Intel's 32nm CMOS technology (Fig.1). Based on this model, the read static noise margin (RSNM) [3] and the write static noise margin (WSNM) [4] of a 6-transistor SRAM are investigated. In this paper, we study the influence of the device DIBL on SNM. As the device DIBL is varied, the off-state current (I_{off}) and the saturation current (I_{dsat}) are kept constant to satisfy the constraints on static power and speed.

3. Results and Analyses

Device DIBL

To address the impact of the device level characteristics on the SRAM behavior, we change the DIBL of the pull down, pull up and access transistors both separately and simultaneously, and simulate the RSNM and WSNM (Fig.2). With identical I_{off} and I_{dsat}, a high-DIBL device has a smaller drain current than a low-DIBL device at the same intermediate biasing conditions. The difference is more significant in the linear-to-saturation transition region.

Switching Trajectory

The switching trajectory of an inverter has been widely used to analyze inverter performance [5]. However, the trajectory of SRAM operations is not yet well investigated. We can analyze the effect of DIBL on SNM through the trajectory. There is a one-to-one relation between the trajectory and the voltage transfer curve of the SRAM. To maximize RSNM, an ideal voltage transfer curve should have zero gain at $V_R>V_{dd}/2$ and $V_R<V_{dd}/2$, and infinite gain at $V_R=V_{dd}/2$, corresponding to the ideal trajectory shown in Fig.3. The actual trajectory deviates from the ideal trajectory, especially at the $V_R>V_{dd}/2$ bias region, in which the trajectory is determined by the saturation region of the access transistor and the linear-to-saturation transition region of the pull down transistor. Since a lower DIBL increases the current in the transition region, reducing the DIBL of the *pull down transistor* is the most effective in improving SRAM stability (Fig.4).

WSNM can be analyzed in a similar way. The write trajectory is mainly determined by the transition region of the access transistor and the saturation region of the pull up transistor (Fig.5). Lowering the DIBL of the *access transistor* is the most effective way to improve WSNM due to the current enhancement in the transition region (Fig.5). We note that the effect of reducing the pull up transistor's DIBL (Fig.6) depends on the ratio of the transistor widths.

WSNM vs. RSNM

Generally, there is a competing effect between RSNM and WSNM, e.g., increasing the size of the access transistor improves WSNM but degrades RSNM. However, because changing the DIBL of the three transistors have different effects on SNM (Fig. 2), improving the DIBL of both the pull-down and the access transistor can simultaneously enlarge RSNM and WSNM (Table. I). This suggests we could improve both RSNM and WSNM by reducing DIBL through device engineering such as optimizing the doping profile, using a thinner channel body, and relaxing the channel length. Moreover, improving the DIBL of the pull up transistor can increase the RSNM and WSNM simultaneously for certain ratios of the widths of the transistors (Table I).

By varying the DIBL and the ratio of the transistor widths, the RSNM and WSNM can be engineered to cover a wide range. The optimum design is on the Pareto optimal curve of Fig.7, e.g., for a design targeting RSNM at 0.17V, the maximum WSNM is achieved by choosing the ratio of the pull down, pull up and access transistors to be 2.5:1:1.5 and the DIBL to be 50, 100, 100mV/V, respectively.

4. Conclusions

Using a device behavioral model, we carefully analyze the effect of DIBL on SRAM read and write static noise margins. A switching trajectory approach is proposed to analyze the impact of the device I-V characteristic on the SNM of a SRAM cell. Reducing the DIBL of the pull down and access transistor can effectively improve SRAM stability. A 12% simultaneous increase in both RSNM and WSNM is demonstrated by reducing the DIBL of the pull down and the access transistors from 150mV/V to 50mV/V.

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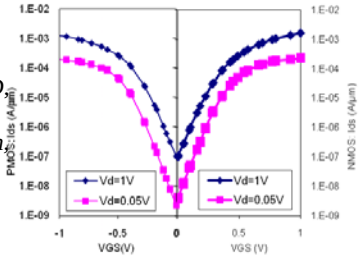

Figure 1 **Model calibration**. Lines are model simulation. Symbols are experimental data

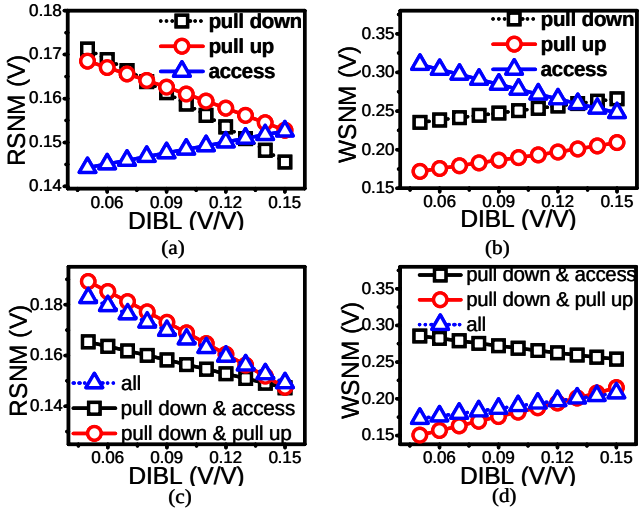

Figure 2 **DIBL vs. SNM**. (a), (b) adjust DIBL of a single transistor. (c), (d) adjust DIBL of multiple transistors for the half cell. In (a), changing pull down is most effective in improving RSNM (17.6%); and in (b) changing access is most effective for WSNM (25.1%).

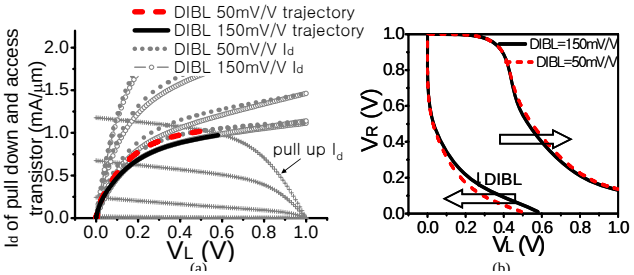

Figure 5 (a) **Write trajectory** for different DIBLs of the access transistor. Low DIBL reduces the V_L of trajectory points at the same V_R biasing and leads to larger WSNM. (b) **Write voltage transfer curve** for different DIBLs of access transistor.

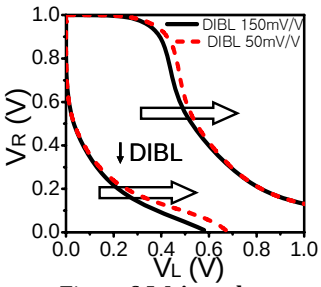

Figure 6 **Write voltage transfer curves** for different DIBLs of pull up transistor.

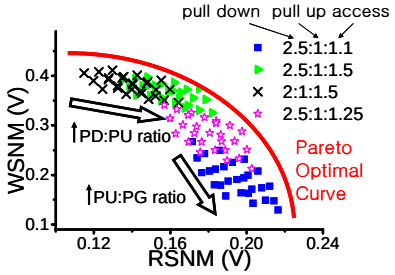

Figure 7 **RSNM vs. WSNM** with different ratios of the widths of transistors (cell area less than 10 times of the pull up transistor's area). Pareto optimal curve are composed of the points that there is no design with both WSNM and RSNM larger than these points.

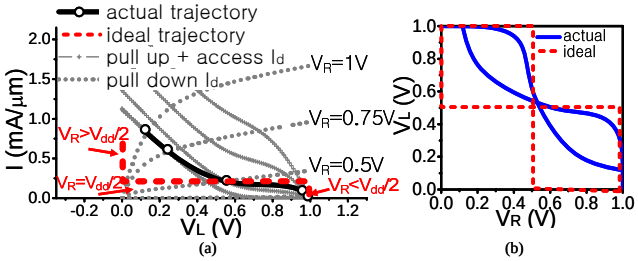

Figure 3 (a) **Read trajectory**. Circles correspond to specific points at V_R=0, 0.25, 0.5, 0.75, 1V biasing conditions. Ideal trajectory has three segments: infinite slope and small V_L at $V_R>V_{dd}/2$ biasing; zero slope at $V_R=V_{dd}/2$ biasing; infinite slope and large V_L at $V_R<V_{dd}/2$ biasing. (b) **Read butterfly curve**.

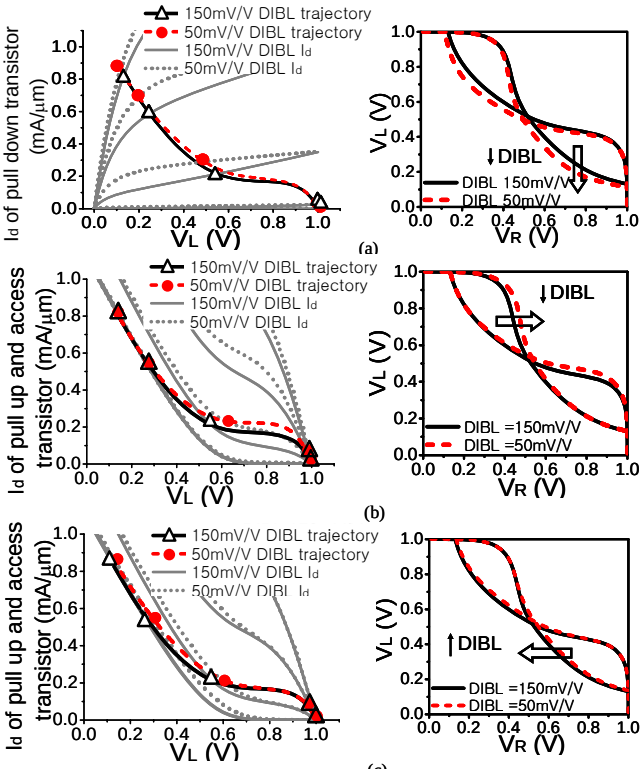

Figure 4 **Trajectory and butterfly curve comparison** with different (a) pull down (b) pull up (c) access transistor DIBL. Circle and triangle are trajectory points at V_R=0, 0.25, 0.5, 0.75, 1V. In (a), low pull down DIBL reduces the V_L of points in the trajectory at the same $V_R>V_{dd}/2$ biasing (up to 20% reduction). In (b), low pull up DIBL increases the slope at $V_R<V_{dd}/2$. In (c), the effect of low access DIBL is similar as (a), but less effective than (a) due to the smaller change of current.

Table I. SNM improvement by reducing DIBL from 150mV/V to 50mV/V on SNM

	Pull down : Pull up : Access ratio and SNM			
	1.5:1:1		2:1:1.5	
	RSNM	WSNM	RSNM	WSNM
Pull Down	+17.6%	-11.4%	+20.1%	-5.31%
Pull Up	+10.3%	-17.8%	**+12.0%**	**+0.63%**
Access	-5.46%	+25.1%	-7.31%	+8.14%
PD+Access	**+12.3%**	**+12.4%**	+12.8%	+2.63%
PU+PD	+28.3%	-30.0%	+32.5%	-6.03%
All	+22.5%	-16.7%	+24.7%	-7.36%