# Ultra-Thin (4nm) Gate-All-Around CMOS devices with High-*k*/Metal for Low Power Multimedia Applications

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#### INTRODUCTION

## It is now commonly admitted that multi-gate or multi-channel devices are the most promising MOSFET architectures to reach ITRS specifications [1] for the end of the roadmap thanks to their superior electrostatic control and their ability to work with undoped channel. Several multi-gate configurations have been proposed in the literature such as FinFET [2,3], Tri-Gate MOSFET [4], multi-channel FET [5], ØFET [6], Gate-All-Around (GAA) [7-11]. In this work, we demonstrate the successful integration of a planar GAA on Silicon-On-Insulator (SOI) substrate using high-k/metal gate stack. This structure, based on the Silicon-On-Nothing (SON) [12] process, is planar self-aligned and allows a very good control of the channel thickness (defined by selective epitaxy). After describing the fabrication process, highlighted by Si-channel integration down to 4nm, electrical results are presented. State-of-the-art performances and excellent DIBL control thanks to the ultra-thin channel thickness are shown.

#### **DEVICES FABRICATION**

Figure 1 illustrates the integration scheme of our device. Starting on a SOI substrate, well implantations with high doses are performed in order to avoid parasitic conduction below the bottom gate (fig. 1-(a)). Then, mono crystalline SiGe / Si / SiGe layers are grown by selective epitaxy (fig. 1-(b)). The two SiGe-layers are sacrificial and determine the future gates position while the Si-layer corresponds to the future conduction channel. A SiN layer is deposited (fig. 1-(b)) and acts as a hardmask during the first gate patterning. The whole stack (SiN/SiGe/Si/SiGe) is then etched with a stop on the initial SOI layer (fig. 1-(c)) directly followed by a silicon epitaxy of the S/D regions to contact the channel (fig. 1-(d)), ensuring thus the self-alignment of the top and bottom gates (fig. 2). Isolation is then performed thanks to the MESA process which permits at the same time a lateral access to the SiGe layers that are selectively removed by CF4 plasma dry etch or hot HCl chemical vapor etch (fig. 1-(e)). These empty cavities are filled with 2.5nm HfO2 high-k dielectric and 10nm TiN metal gate using Atomic Layer (ALD) techniques. The remaining empty space is then filled with polysilicon (fig. 1-(f)). External gates that connect the surrounding gate were then patterned. Conventional spacer, S/D implantation, Rapid Thermal Anneal and silicidation are performed before the standard contact formation and the metal line realization. Figure 3 shows a TEM cross-section of the final structure of our GAA device along the gate length (L) and the gate with (W). The TEM cross-section along the gate width in fig.4 highlights our gate surrounding a very thin channel down to 4nm.

#### **ELECTRICAL RESULTS**

In order to prevent from any parasitic conduction between the bottom gate and the Buried Oxide (BOX), we performed high dose implantations. The doping profile "as implanted" was used to simulate the characteristics of the bottom parasitic channel (fig. 5). The simulated  $I_D(V_G)$  (fig. 5) curves confirm a very high threshold voltage ( $V_T$ =0.97V) for the bottom transistor. This clearly means that no significant parasitic conduction will occur below the bottom gate for  $V_G \leq 1V$ . This was also confirmed on measured  $I_D(V_G)$  (fig. 6) with various backbiasing. No change in the characteristic was observed for substrate polarization down to -50V.

40nm x 47nm (LxW) GAA show excellent drive current. Un-normalized drive currents is 75µA for NMOS and 30µA for PMOS. By normalizing by footprint our GAA devices exhibit excellent performances with ION=1600µA/µm @  $I_{OFF}0.8nA/\mu m$  for NMOS and  $I_{ON}=640\mu A/\mu m$  $I_{OFF}0.2nA/\mu m$  for PMOS at  $|V_{DD}|=1V$ . The corresponding effective currents are IEFF=758/334 µA/µm for N/P MOS respectively. The double gate configuration allows a very low DIBL values lower than 25mV for NMOS and than 30mV for PMOS and very abrupt sub-threshold slope of 69 mV/dec for both N and PMOS devices (fig. 7).  $I_D(V_D)$ characteristics are shown in fig. 8. With its thin channel, our GAA confirms very good electrostatic immunity: no roll-off is observed on the  $V_T(L_G)$  curve (fig. 9) and the DIBL vs.  $L_G$ (fig. 10) shows that the GAA is the ideal structure to control short channel effects compared to the single gate FDSOI reference [13].

Figure 12 proposes a benchmark of the best multi-gate (FINFET, Tri-Gate, MCFET,  $\Phi$ FET and GAA) performances reported so far. To provide a comparison as fare as possible, all currents are normalized by the channel perimeter. For our devices, according to fig. 4, we assume the perimeter to be two times the channel width. Our GAA presents performances among the best published in the literature.

### CONCLUSION

We successfully fabricated high-k/metal planar self-aligned GAA CMOS devices relying on SON process. With its surrounding gate, the GAA presents excellent electrostatic control and very good sub-threshold characteristics. It also exhibits high-drive current at low standby current confirming the potential of GAA architectures for 16nm node and below.

**References :** [1] http://www.itrs.net/ [2] Vellianitis *et al.*, IEDM 2007. [3] Chang *et al.*, IEDM 09 [4] Kavalieros *et al.*, VLSI 2006. [5] Bernard *et al.*, VLSI 2008. [6] Dupré *et al.*, IEDM 2008. [7] Li *et al.*, VLSI 2009. [8] Bungsaruntip *et al.*, IEDM 2009. [9] Wong *et al.*, VLSI 2009. [10] Bidal *et al.*, VLSI 2009. [11] Pouydebasque *et al.*, Silicon Nanoelectronics Workshop 2007. [12] Jurczack *et al.*, IEEE-TED, p2179, 2000. [13] Fenouillet *et al.*, ESSDERC 2009



Fig. 1: Illustrations of the integration scheme

Si Channel:

Surrounding gate

=47nm T<sub>s</sub>

Fig. 4: TEM cross-section along the gate width allows

SiN Hardmask



Fig. 2: TEM cross-section after Si epitaxy of S/D regions (step d). The SiGe marker shows the stop of the first gate etch (step c). The two future gates (here represented by the SiGe layers) are self-aligned thanks to this process.



Fig. 3: TEM cross section along the gate length (L) and along the gate width (W) showing the final structure of the GAA planar device. The silicon channel is well contacted by the S/D epitaxied regions. This TEM also confirms the successful integration of the self-aligned process with equal L<sub>G</sub>=40nm for both top and bottom gate.



seeing that surrounding gate process can pe performed Fig. 5: Well implant profile simulation. The corresponding bottom channel MOSdown to ultra thin silicon channel (Tsi=4nm) and the FET is simulated. I<sub>D</sub>-V<sub>G</sub> curves show that the bottom channel has a threshold voltage of 0.97V.



Fig. 6: I<sub>D</sub>-V<sub>G</sub> characteristics with substrate polarization down to Vb=-50V revealing no parasitic conduction channel.



Fig. 9: V<sub>T</sub> vs. L<sub>G</sub> evolution shows no roll-off. Confirming the excellent control of short channel effects of the GAA.



Fig. 7: ID-VG curves for NMOS and PMOS GAA devices normalized by footprint. Excellent performances and very good sub-threshold behavior is observed.



Fig. 10: DIBL vs. LG shows excellent DIBL control of the GAA for short gate length compared to single gate FDSOI reference.



Fig. 8: ID-VD characteristics of 40nm gate length GAA devices. Performances are normalized by design footprint.



Fig.11: Benchmark of all the best performances reported so far on multi-gate architectures. Our planar GAA (black dots) is among the best state-of-the-art.

