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Heavily-Doped Poly-Si Gate and Epi-First Source/Drain Extension Technique in Strained Si Nanowire MOSFETs with Reduced Parasitic Resistance

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1. Introduction

Nanowire field-effect-transistors (NW FETs) are regarded as promising candidates for ultimate scaling [1]. In order to obtain high performance NW FETs for practical use, reducing parasitic resistance (R_{SD}) [2,3] and enhancing inversion-layer mobility (μ) [4] are essential (Fig.1). We reported the large R_{SD} reduction by means of raised source/drain (S/D) extensions with thin gate spacer, achieving higher I_{on}/C_{inv} than the previous NW FETs with epi S/D [5]. However, further R_{SD} reduction is still required for high performance Si LSI. For μ enhancement, on the other hand, applying strain to NW channel region is necessary in addition to the surface orientation engineering [6]. However, the μ enhancement technique for NW FETs is still insufficient.

In this paper, we demonstrate further I_{on} improvement by *Epi-first* S/D extension process. In addition, we successfully obtained I_D enhancement due to the compressive strain applied from heavily-doped poly-Si gate.

2. NW FETs Fabrication

Tri-gate NW FETs were fabricated on (100) SOI wafers. Fig.2 shows the key process flow. Channel direction/side-surface-orientation is <110>/(110) or <100>/(100). Gate stack is composed of poly-Si and SiO_2 with T_{OX} of 3 and 4nm. Gate pre-doping with high or low dose were performed. The dopants were P, As, and B. After definition of gate and SiN offset spacers, selective epitaxial growth (SEG) of Si on NW S/D was performed prior to extension ion-implantation (Ext. I/I), which we call *Epi-first* S/D extension process. Figs.3(a) and (b) show TEM images of <110> NW channel and S/D region with SEG, respectively. While the conventional *Ext. I/I-first* S/D process like bulk planar FETs requires low dose and low energy ion-implantation to keep crystallinity of Si NW S/D, defect-free S/D SEG was successfully fabricated through the *Epi-first* S/D extension process even with high dose and high energy ion-implantation.

3. Results and Discussion

A. Epi-first S/D Extension

Fig.4 shows I_D-V_G characteristics with V_D of 10 mV. I_D of *Epi-first* NW FETs has 1.8 times higher than that of the conventional *Ext. I/I-first* NW FETs. In R_{lin}-L_G plots (Fig.5), R_{lin} of *Epi-first* NW FETs is smaller than that of *Ext. I/I-first* NW FETs. It is also confirmed that the variability of R_{lin} is suppressed in *Epi-first* NW FETs with short L_G, because SEG of S/D was uniformly formed. High dose and high energy Ext. I/I in *Epi-first* NW FETs fabrication leads to the low-resistivity extension region with large amount of dopants (Fig.6). The fact suggests that effective gate length (L_{eff}) of *Epi-first* NW FETs was shortened against L_G due to thin gate spacer used in this experiment. In order to compare the R_{lin} under the same short-channel-effect (SCE), Fig.7 shows the relationship between R_{lin} and DIBL. As DIBL becomes large, R_{lin} decreases drastically due to the reduction of the channel resistance. The minimum R_{lin} of *Epi-first* NW FETs, which is almost corresponding to R_{SD}, is lower than that of *Ext. I/I-first* NW FETs. At the same DIBL of 100 mV/V, 37% R_{lin} reduction was achieved in *Epi-first* NW FETs. Furthermore, 40% I_{D_lin} enhancement was obtained at I_{off} of 1 nA/μm (Fig.8). These results indicate that *Epi-first* S/D extension process to increase S/D impurity is indispensable process for large R_{SD} reduction of short-channel NW FETs. Therefore, low R_{SD} and acceptable SCE could be realized by optimizing the spacer width in the *Epi-first* NW FETs. In I_{on}-I_{off} plots (Fig.9), I_{on} of the *Epi-first* NW FETs increases 20% at I_{off} of 1 nA/μm.

B. Heavily-doped Poly-Si Gate

Fig.10 shows I_D-V_G characteristics of Si NW FETs with high- and low-doped poly-Si gate. These NW FETs were fabricated on the same wafer with changing gate pre-doping conditions to eliminate the wafer-to-wafer fluctuation. It is found that the I_D of As- and P-doped poly-Si gate are higher than that of B-doped gate despite the same dose. Furthermore, I_D of the As- and P-doped gate are increased by heavy doping, while no enhancement is observed in NW FETs with heavily-B-doped gate. In the W_{NW} dependence of the I_D enhancement (ΔI_D) of high- to low-dose gate (Fig.11), ΔI_D increases with narrow W_{NW} less than 40nm. ΔI_D also increases with short L_G (Fig.12).

Fig.13 shows the ΔI_D of <110> and <100> NW FETs. The W_{NW} dependence of the ΔI_D shows the same tendency in both channel direction. It is found that ΔI_D in <110> is larger than that in <100>, suggesting the channel direction dependence of ΔI_D induced by the strain. Fig.14 shows the μ change by 0.1% normal compressive strain to top NW surface and 0.1% horizontal compressive strain to side surfaces extracted from substrate bending [5]. While the μ change of top surface in both <110> and <100> nFETs are the same, (110) side surface has large μ increase. The higher ΔI_D in <110> nFET than that in <100> nFETs suggests As- and P-doped poly-Si gate induce the compressive strain to the NW channel. ΔI_D increase against W_{NW} (Fig.11) means the strain enhancement in narrow W_{NW}. In cross-sectional TEM image of NW FETs (Fig.15), the poly-Si grain boundary is observed at the corner to surface. As reported [7], high P concentration forms the vacancy in Si lattice and excess Si atoms stabilize at grain boundary or surface. The re-growth of poly-grain could induce outward stress, leading to the compressive stain to the NW channel.

Moreover, tensile-stress liner was formed in heavily-doped poly-Si NW FETs. It is confirmed that the tensile-stress liner enhances I_D of NW nFET with the low-dose gate (Fig.16). In L_G dependence of I_D enhancement ratio (ΔI_D) by tensile stress liner with As- and B-doped gate (Fig.17), As-doped gate NW nFETs becomes larger than B-doped gate at short L_G. ΔI_D of As-doped poly-Si gate is slightly higher than that of B-doped one, irrespective of W_{NW} (Fig.18). Fig.19 summarizes the I_D enhancement due to the tensile-stress liner and the heavily-doped poly-Si gate. The I_D enhancement is extracted from the I_D difference from the NW FETs with B-doped poly-Si gate and neutral liner. It is found that longitudinal tensile strain by the stress liner and vertical compressive strain by heavily-doped poly-Si gate are additive and 43% I_D enhancement is achieved in short L_G.

Conclusions

We achieved R_{SD} reduction and I_{on} enhancement in NW FETs with *Epi-first* process and compressive stress induced by heavily-doped poly-Si gate. 20% I_{on} enhancement was obtained compared to conventional *Ext. I/I-first* process. Heavily-doped poly-Si gate process is additive to tensile stress liner. This stress technique can be applicable to poly-Si/metal stacked gate NW FETs.

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References:[1] K.H.Yeo et al.**,** IEDM2006, p.539**.** [2] H.S.Wong et al.,VLSI2009, p.92. [3] S.Bangsaruntip et al., IEDM2009, p.297. [4] J.Chen et al., VLSI2008, p.32. [5] M.Saitoh et al., to be presented at VLSI2010. [6] M.Saitoh et al., VLSI2008, p.18. [7]A.F.W.Willoughby, "Double-Diffusion Process in Silicon" in F.F.Y.Wang, Ed., Impurity Doping Process in Silicon (1981).

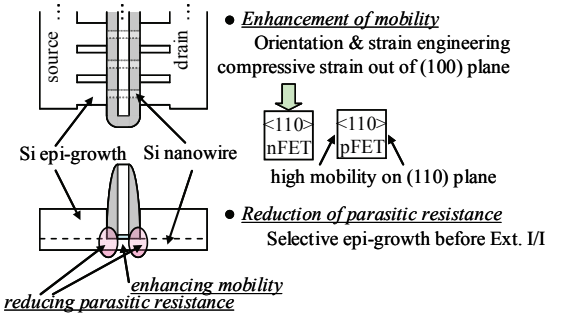

Fig.1 Schematics of top and cross-sectional view of nanowire FETs. Mobility enhancement and resistance reduction are required.

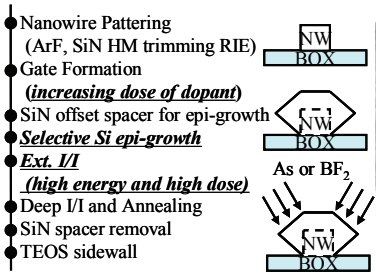

Fig.2 Key process flow for *Epi-first* S/D and heavily-doped Poly-Si gate.

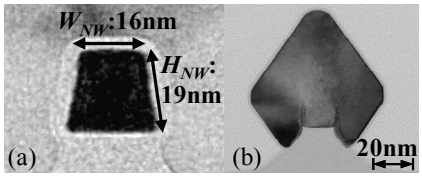

Fig.3 Typical cross-sectional TEM images: (a) nanowire and (b) S/D after epi. Si NW with NW height (H_{NW}) and width (W_{NW}) of 19nm and 16nm was successfully fabricated.

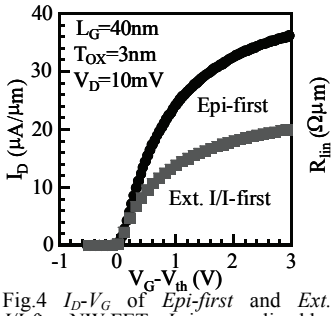

Fig.4 I_D-V_G of *Epi-first* and *Ext. I/I-first* NW FETs. I_D is normalized by circumference (W_{NW}+2*H_{NW}).

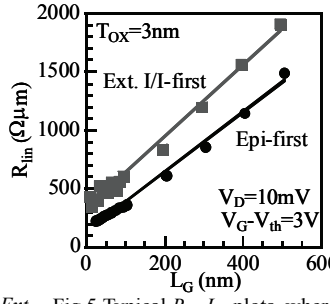

Fig.5 Typical R_{lin}-L_G plots, where L_G is defined as gate ploy-Si length.

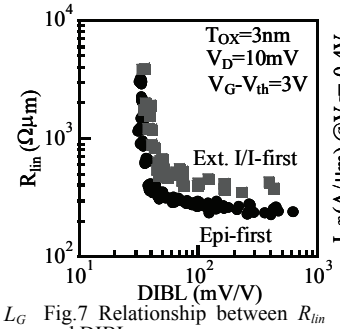

Fig.7 Relationship between R_{lin} and DIBL.

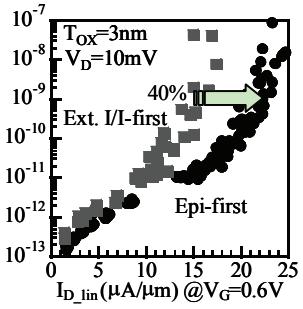

Fig.8 I_{D_lin}-I_{off} plots of nanowire FETs. 40% I_{D_lin} enhancement is achieved at I_{off} of 1nA/μm.

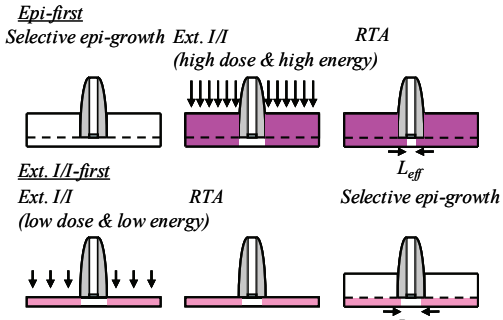

Fig.6 Schematics of *Epi-first* and *Ext. I/I-first* processes.

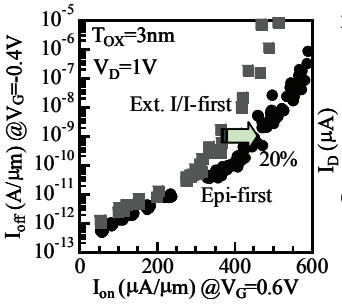

Fig.9 I_{on}-I_{off} plots of nanowire FETs. 20% I_{on} enhancement is achieved at I_{off} of 1nA/μm.

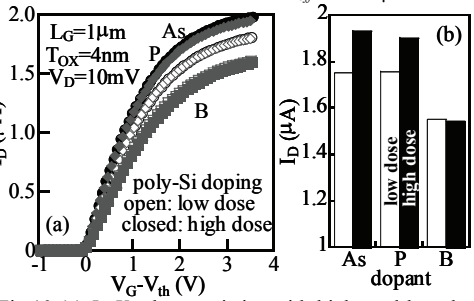

Fig.10 (a) I_D-V_G characteristics with high- and low-doped gate. (b) I_D at V_G-V_{th} of 3V. H_{NW}=14nm. W_{NW}=21nm.

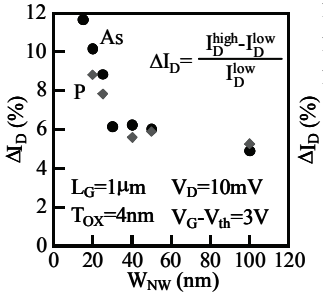

Fig.11 W_{NW} dependence of I_D enhancement of high- to low-dose gate NW FETs.

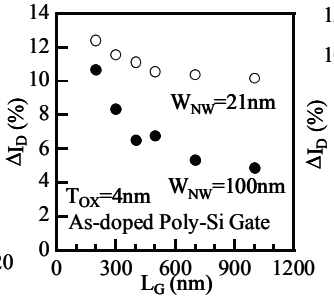

Fig.12 L_G dependence of I_D enhancement of high- to low-dose gate NW FETs.

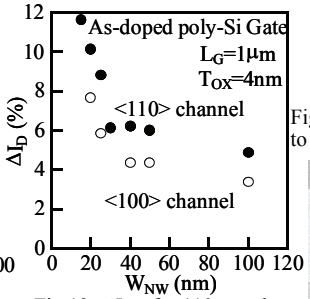

Fig.13 ΔI_D of <110> and <100> channel NW FETs. H_{NW}=21nm in <100>.

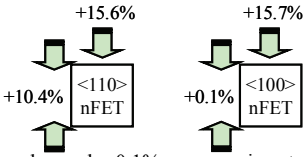

Fig.14 μ change by 0.1% compressive strain normal to top surface and horizontal to side surface.

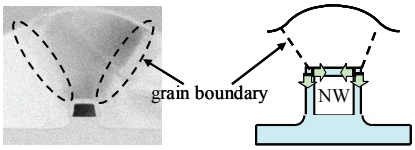

Fig.15 Cross-sectional TEM image of NW FETs Poly-Si grain boundary at the corner could induce outward stress.

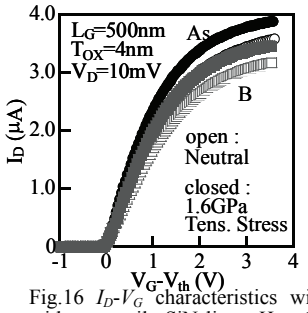

Fig.16 I_D-V_G characteristics with or without tensile SiN liner. H_{NW}=14nm. W_{NW}=21nm.

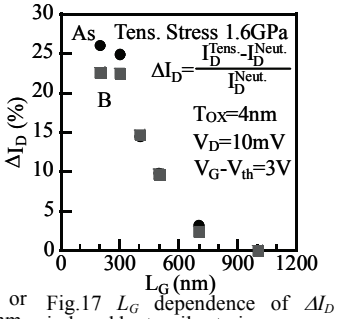

Fig.17 L_G dependence of ΔI_D induced by tensile strain.

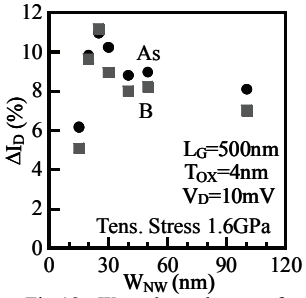

Fig.18 W_{NW} dependence of ΔI_D by tensile strain.

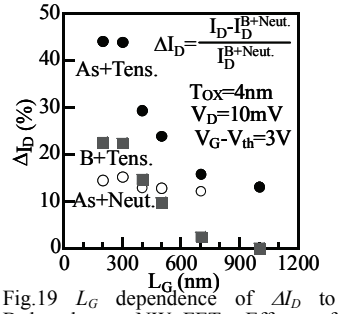

Fig.19 L_G dependence of ΔI_D to B-doped gate NW FETs. Effects of As-doped and tens. strain is additive.