Low GIDL and Its Physical Origins in Si Nanowire Transistors

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Abstract

Gate-induced drain leakage (GIDL) in Si nanowire (NW) transistors fabricated on SOI substrates is systematically studied. GIDL current ($I_{GIDL}$) is drastically reduced in NW FETs with the NW width ($W_{NW}$) of around 10 nm, which realizes extremely small off-current ($I_{off}$) devices. The reduction of local electric field around the drain junction due to low impurity concentration in source/drain (S/D) extensions and the relatively large S/D parasitic resistance are identified as the main mechanisms of small $I_{GIDL}$.

1. Introduction

NW FETs are promising devices for further scaling due to their excellent short-channel performance and low sub-threshold leakage current ($I_{sub-leak}$) [1]. One of the major leakage current components in scaled MOSFETs is GIDL that is caused by band-to-band tunneling at the gate/drain (G/D) overlap region (Fig. 1) [2–4]. Although it is important to suppress GIDL for low-power technologies, no systematic study has been reported on GIDL in NW FETs.

In this work, we present significant reduction of GIDL in narrow NW FETs for the first time. Evaluating the effective length of the G/D overlap region ($L_{ov}$) and S/D parasitic resistance ($R_{SD}$), we clarify the origin of low GIDL in narrow NW FETs.

2. Devices

We have fabricated tri-gate NW FETs on (100) SOI wafers with a 24 nm-thick SOI film. Poly-Si gate/4nm-SiO2 is used as gate stacks. To reduce $R_{SD}$, raised S/D with 25-mm-thick epi-Si are employed. Figure 2 shows the cross-sectional TEM images of a NW FET with the NW width ($W_{NW}$) of 15 nm and $L_{G}$ of 30 nm.

3. GIDL in NW FETs

Figure 3 shows $I_{D}-V_{G}$ of NW nFETs with $W_{NW}$ of 30 nm. $I_{D}$ is normalized by the circumference ($W_{NW} \times 2 \times H_{NW}$), and $V_{D}$ is 1 V. $I_{off}$ at the fixed gate overdrive ($V_{G}=V_{TH}-3$ V) are plotted in Fig. 4. Larger $I_{off}$ caused by GIDL is obtained in short-channel NW FETs. It is due to the parasitic bipolar junction transistor (BJT) effect, and the BJT gain is almost comparable to that reported in planar-SOI FETs [3].

Figure 5 shows $I_{D}-V_{G}$ of NW nFETs with various $W_{NW}$. $L_{G}$ is 10 μm and $V_{D}$ of 2 V is applied. $I_{GIDL}$ is strongly dependent on $W_{NW}$, and two remarkable tendencies are obtained. Firstly, the $V_{G}$ where $I_{GIDL}$ exceeds $I_{sub-leak}$ shifts in a positive direction as $W_{NW}$ decreases. This $V_{G}$ is defined as $V_{GD}$ in this paper, and $\Delta V_{GD}$, which is defined as $\Delta V_{GD}(W_{NW})=V_{GD}(W_{NW})-V_{GD}(W_{NW}=100 \text{ nm})$, is plotted in Fig. 6. $W_{NW}$ dependence of $\Delta V_{GD}$ is comparable in both pFETs and nFETs, which indicates that the shift of $V_{GD}$ is related to the structural feature of NW. In narrow NW FETs, $V_{GD}$ offers better electrostatic control and thus the channel potential just under the gate is more effectively lowered than in wide NW FETs, therefore narrower NW FETs show larger $I_{GIDL}$ even where $V_{GD}$ is relatively small.

Secondly, the variations in $I_{GIDL}$ against $V_{G}$ (i.e. $dI_{GIDL}/dV_{G}$) become smaller as $W_{NW}$ decreases. As a result, quite small $I_{off}$ is realized when $V_{GD}$ is sufficiently smaller than $V_{T}$ in narrow NW FETs. Figure 7 shows normalized $I_{off}$ as a function of $W_{NW}$ at $V_{G}=V_{TH}-2$ V. Particularly, nFETs show strong reduction in $I_{off}$; $I_{off}(W_{NW}=10 \text{ nm})$ is smaller than $I_{off}(W_{NW}=100 \text{ nm})$ by three orders of magnitude.

4. Changes in $L_{ov}$ and $R_{SD}$

Since GIDL is induced by the band-to-band tunneling around the drain extension, the impurity concentration and its distribution in extensions have a great impact on GIDL.

We have estimated $L_{ov}$ from the $L_{G}$-dependence of the gate-channel capacitance that is measured by split-CV. It is plotted as a function of $W_{NW}$ in Fig. 8. $L_{ov}$ decreases as $W_{NW}$ becomes smaller in both nFETs and pFETs.

$R_{SD}$ is extracted from the y-intercept of $R_{SD}-L_{G}$ at high $V_{G}$. As shown in Fig. 9, $R_{SD}$ is relatively high particularly in nFETs with small $W_{NW}$.

5. Discussions

Reduction of $dI_{GIDL}/dV_{G}$ at small $W_{NW}$ is attributed to the changes in the extension profile because the degree of reduction depends on the extension dopant species as shown in Fig. 7. $L_{ov}$ reduction (Fig. 8) indicates that the impurity concentration of extensions in smaller-$W_{NW}$ NW FETs is lower possibly due to dopant loss during ion implantation into narrow silicon structures [5]. As a result, the gradient of impurity concentration around the drain junction becomes low. It causes the reduction of local electric field, resulting in suppression of GIDL.

Large $R_{SD}$ also reduces the electric field in a drain junction because it causes large voltage drop, which modulates the potential in a drain junction ($V_{GD}$) as shown in Fig. 10. Increase in $R_{SD}$ is more significant in nFETs than pFETs, which agrees with larger reduction of GIDL in nFETs.
6. Conclusion
We have systematically studied GIDL in NW FETs fabricated on SOI substrates. By reducing $W_{NW}$, $dI_{GIDL}/dV_G$ rapidly decreases. It is attributed to the decrease in local electric field at the drain junction. Small-$W_{NW}$ FETs are effective in reducing $I_{GIDL}$, as well as sub-threshold leakage, which means NW FETs are suitable for ultra-low-power applications.

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References

Fig. 1: (a) A schematic illustration of G/D overlap region in nFETs. (b) The energy band diagram.

Fig. 2: Cross-sectional TEM images of (a) gate-length direction and (b) width direction.

Fig. 3: (a) $I_G-V_G$ of NW nFETs with $W_{NW}$ of 30 nm.

Fig. 4: $I_{DS}$ at $V_G$=$V_T$-3 V as a function of $L_G$.

Fig. 5: (a) $I_G-V_G$ of NW nFETs with various $W_{NW}$. (b) Detailed plots where GIDL is clearly observed.

Fig. 6: $\Delta V_{G0} \left(V_{G0}(W_{NW}) - V_{G0}(W_{NW}=100 \text{ nm})\right)$ as a function of $W_{NW}$.

Fig. 7: $I_{DSS}$ at $V_G$=$V_T$-3 V normalized to $I_{DSS}(W_{NW}=100 \text{ nm})$ as a function of $W_{NW}$.

Fig. 8: Effective length of the G/D overlap region ($L_{ov}$) as a function of $W_{NW}$.

Fig. 9: S/D parasitic resistance ($R_{SD}$) as a function of $W_{NW}$.

Fig. 10: Schematic illustration of $R_{SD}$, $R_{SD}$ modulates the potential in a drain junction ($V_{jet}$).