Extended Abstracts of the 2010 International Conference on Solid State Devices and Materials, Tokyo, 2010, pp1008-1009

C-6-1(Invited)

Extremely-Thin SOI for Mainstream CMOS: Challenges and Opportunities

A. Khakifirooz, K. Cheng, A. Kumar, P. Kulkarni, S. Ponoth, B. S. Haran, S. Mehta, J. Cai, A. Bryant, J. Kuss, L. F. Edge, H. Jagannathan, Z. Ren, A. Reznicek, T. Adam, H. He, A. Kimball, S. Kanakasabapathy, S. Schmitz, S. Holmes, A. Majumdar, B. Jagannathan, D. Yang, A. Upham, S.-C. Seo, J. L. Herman, R. Johnson, Y. Zhu, P. Jamison, Z. Zhu, L. H. Vanamurth, J. Faltermeier, S. Fan, D. Horak, T. Hook, V. Narayanan, V. Paruchuri, H. Bu, D. K. Sadana, P. Kozlowski, B. Doris, D. McHerron, W. Haensch, M. Khare, E. Leobondung, J. O'Neill, and G. Shahidi

IBM Research, Albany, NY 12203
E-mail: khaki@us.ibm.com

1. Introduction

Extremely thin SOI is considered as one of the promising candidates for scaling to 20nm node and beyond. Superior short channel control without need to aggressive scaling of the gate dielectric or channel doping and immunity to random dopant fluctuation in undoped channel make this device structure attractive [1]. Unlike FinFET or other 3D structures, ETSOI is a planar structure and thus device fabrication and process characterization are much easier. Moreover, the fact that electrical characteristics of the device can be adjusted by the voltage or doping under the BOX, opens new opportunities for V_T tuning [2], power management, and embedded non-volatile memories [3].

2. ETSOI Integration

Since silicon layer is extremely thin (6nm or smaller to maintain device electrostatics), any silicon loss during device processing is not acceptable. Also, a low-damage junction formation process should be used that avoids full amorphization of the S/D region. Ion implantation either through raised S/D [4] or with a disposable spacer [5] has been proposed in the past, but scalability of these approaches to very thin Si channels is a challenge.

We have developed an integration scheme that uses dopant drive-in from in-situ doped RSD to form the extension [1] and thus avoids any implant damages. Devices with channel thickness less than 2 nm can be realized with this process (Fig. 1). Conventional epitaxy pre-clean process leads to significant Si agglomeration (Fig. 2). Thus, a low-temperature pre-clean process was developed. Fig. 3 shows more than 3 orders of magnitude reduction in the chain resistance obtained with the optimized process. As shown in Fig. 4, optimization of the epitaxy process is critical to yield narrow channel devices with good performance.

Fig. 5 shows a TEM cross section of the ETSOI MOSFET with a gate length of 25 nm and channel thickness of 6 nm. A raised source/drain structure is needed to contact the thin silicon channel. However, the RSD structure increases the total transistor parasitic capacitance. This is especially a concern for future technology nodes, where parasitic capacitance dominates the total transistor load. We have developed a faceted epitxy process to reduce the parasitic capacitance. The epitaxy process is tuned to form (111) facets as opposed to (311) facets in order to enable adequate RSD thickness in future technology nodes. Fig. 6 shows TCAD simulation results indicating that 15% reduction in the total parasitic capacitance is achieved at a given series resistance if a faceted epitaxy is used instead of the conventional vertical RSD [1].

3. Device Performance

Figs. 7 and 8 show the performance of the low-power and high-performance NFETs and PFETs, respectively. With V_{DD}=0.9 and at I_{off}=1nA/μm, NFET and PFET transistors have a drive current of 650 and 480 μA/μm, respectively. High-performance devices have a drive current of 870 and 660 μA/μm for NFET and PFET, respectively and at I_{off}=100nA/μm. PFET performance is in particular respectable owing to small series resistance (R_{ext} < 170 Ω.μm) obtained by in-situ doped SiGe RSD and implant-free extension formation.

Fig. 9 shows the RF performance of the ETSOI devices. NFET and PFET transistors demonstrate a cut-off frequency of 300 and 260 GHz, respectively, with L_G=25 nm and contacted gate pitch of 260 nm [3]. No substrate contact is required for analog and RF devices due to the absence of history effect in fully-depleted transistors.

Analog devices are critical for SoC applications. The performance of analog devices is strongly driven by device matching, linearity, and g_m/g_{ds} ratio. Fig. 10 shows the g_m/g_{ds} characteristics of the analog devices with thin and thick oxide as a function of the gate length. Significant self-gain is achieved at gate length down to 25 nm.

4. Local and Global Variation

Device variation is a major concern in future technology nodes. We have demonstrated record device matching with ETSOI device [1] as shown in Fig. 11. Silicon thickness variations is believed to be one of the sources of global variation in ETSOI. Fig. 12 shows the correlation between short-channel VT and the estimated channel thickness demonstrating a sensitivity of 25 mV/nm. These results provide a guideline for silicon thickness uniformity across the wafer.

References

[1] K. Cheng, *et al.*, *IEDM Tech. Dig.*, p. 49, 2009.
[2] M. Khater, *et al.*, *Symp. VLSI Tech.*, p. 43, 2010.
[3] R. Ranica, *et al.*, *IEEE Trans. Nanotechnology*, p. 581, 2005.
[4] C. Fenouillet-Beranger, *et al.*, *IEDM Tech. Dig.*, p. 267, 2007.
[5] A. Majumdar, *et al.*, *IEEE Electron Device Lett.*, p. 413, 2009.

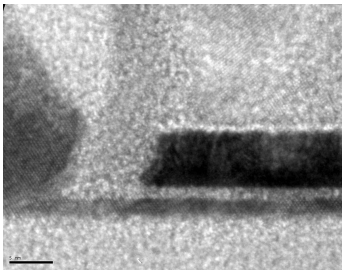

Fig. 1 TEM cross section of the ETSOI device with a channel thickness of 1.9 nm.

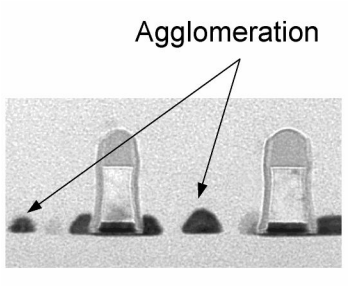

Fig. 2 TEM cross section showing agglomeration with non-optimized epitaxy process.

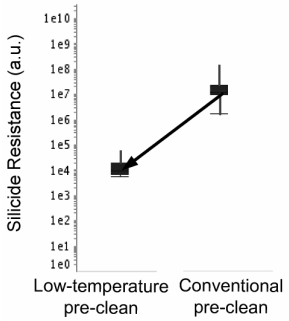

Fig. 3 Significant reduction in silicide resistance indicates that low-temperature pre-clean is needed to avoid agglomeration.

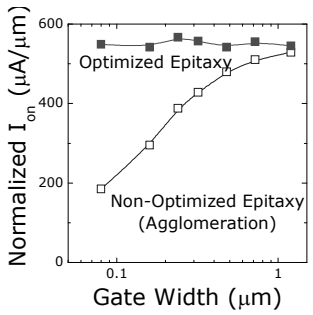

Fig. 4 Drive current at constant overdrive showing the importance of epitaxy optimization to avoid agglomeration in narrow devices.

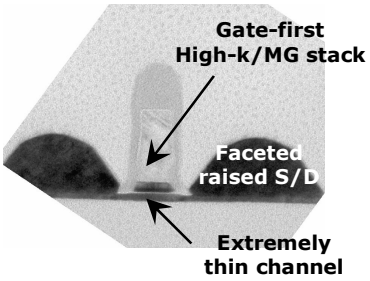

Fig. 5 TEM cross section of the ETSOI device.

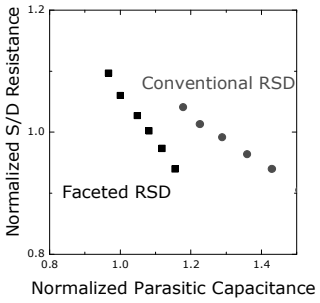

Fig. 6 TCAD simulations showing 15% reduction C_{para} by faceted RSD at a constant R_{ext} [1].

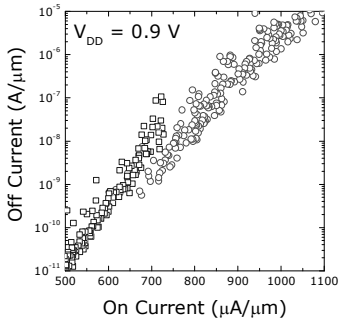

Fig. 7 I_{on}-I_{off} characteristics of LP and HP NFETs showing drive current of 650 and 870 μA/μm at I_{off} = 1 and 100 nA/μm off current, respectively.

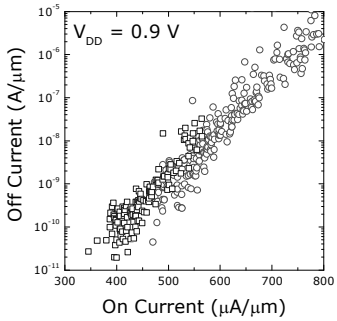

Fig. 8 I_{on}-I_{off} characteristics of LP and HP PFETs showing drive current of 480 and 660 μA/μm at I_{off} = 1 and 100 nA/μm, respectively.

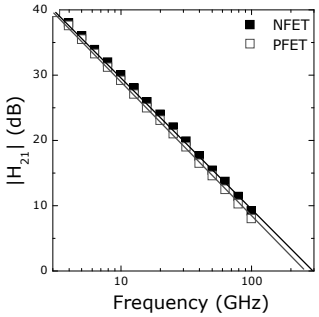

Fig. 9 ETSOI NFETs and PFETs with L_G=25 nm and CPP = 260 nm show f_T of 300 and 260 GHz, respectively.

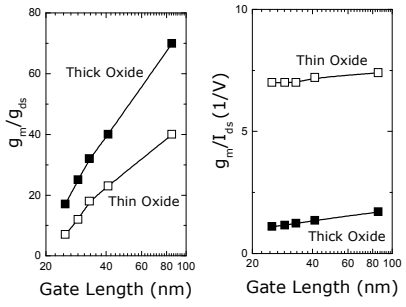

Fig. 10 Excellent analog operation is possible down to L_G=25 nm and without need to special design [1].

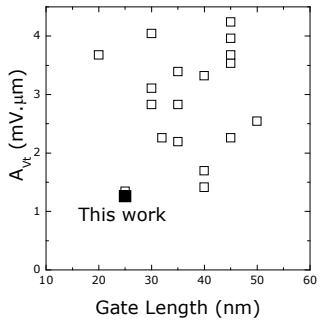

Fig. 11 Record device matching is achieved in ETSOI devices with undoped channel [1].

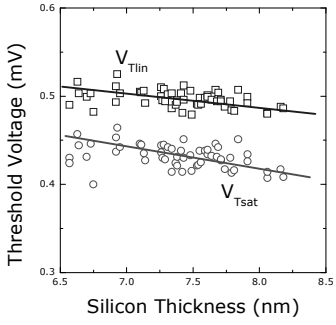

Fig. 12 Correlation between channel thickness and short channel V_T showing 25 mV/nm sensitivity.