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Variability in Variable-Body-Factor Silicon-on-Thin-Box MOSFETs (SOTB MOSFETs)

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Introduction

SOTB (silicon on thin box) MOSFET presents an excellent immunity to SCEs (short channel effects) regardless of low or even intrinsic channel doping concentration. As a result, reduced RDF (random dopant fluctuation) and enhanced mobility can be obtained. Together with proper back-gate bias scheme (to control the threshold voltage and power consumption), SOTB may be an attractive choice for some nano-scale applications (e.g. ultra-low standby-power application) [1]. However, it also has some disadvantages like large parasitic capacitance, especially when ground plane (GP) is adopted to suppress the DIBL effect. Variable-body-factor (or variable-γ) SOTB is a new device concept proposed by [2], which uses a side-gate bias to control body-factor (γ) to obtain a better performance (e.g. reduced parasitic capacitance and improved drive current, .etc) compared to conventional SOTB. The introduction of side-gate has a drawback of enlarged area, which can be minimized by layout design [2]. Besides, it also disturbs the device's variability performance, which has not been studied yet. In this work, we systematically investigated the influences of LER (line-edge-roughness), WFV (work-function variation) and STV (silicon-layer thickness variation) on 20-nm-gate SOTB MOSFETs. Since intrinsic channel has been used, RDF is not considered here.

Simulation Method

Fig.1 (a) shows the simulated variable-γ SOTB MOSFET structures. Fig.1 (b) shows the metal gate work-functions of different grain orientations. Corresponding device parameters are listed in Fig.1 (c). Fig.1 (d) illustrates the fluctuation sources respectively. A Fourier analysis of the power spectrum of Gaussian autocorrelation function is employed to simulate LER (Δ=1.5nm and Λ=20nm) [3]. The silicon layer thickness tolerance is taken as 10% [4]. The work-function distribution is modeled as a probabilistic one, as explored in [5][6]. The ISE TCAD tools [7] have been used to implement our simulations, each of which has a sample size of 100. Quantum effect is taken in to account by the density-gradient method. The threshold voltage is extracted by the constant current method (1.5 $x10^{-7}$A and 0.5 $x10^{-7}$A for n and p channel devices, respectively).

Results and Discussion

Fig.2 shows the tuning effect of side-gate bias on body-factor (simply defined as $|\Delta V_{tsat}/\Delta V_{back\text{-}gate}|$ or C_{body}/C_{gate} [2]) of n-SOTB. When the side-gate is positive biased, it will collect the inverted carriers under the box (electron for n-SOTB) and thus keeps the substrate depleted, leading to a reduced γ as well as lowered threshold voltage (V_{th}). The circled two points donate the selected work state (standby/active state [2]) in this work. Fig.3-5 show fluctuations of V_{tlin} (active state V_{th} extracted at $|V_{ds}|$=0.05 V), V_{tsat} (active state V_{th} extracted at $|V_{ds}|$=0.9V) and DIBL ($|V_{tlin}- V_{tsat}|/0.85$). Dashed lines indicate values of conventional SOTB MOSFETs. As we can see, WFV dominates σV_{tlin} while LER stands out at high drain bias, both for n- and p-SOTB, indicating that LER causes a strong fluctuation of DIBL as illustrated in Fig.5. A comparison between variable-γ and conventional SOTB demonstrates that side-gate bias reduces the V_{th}-roll-off (see Fig.3) while, however, causes a larger σDIBL (see Fig.5) at active state. This is because the side gate helps to deplete the substrate, and thus reduces the charge share effect. Meanwhile, the depleted substrate strengthens the fringing field induced by drain and source through the buried box and substrate [8], leading to a deteriorated DIBL. Fig.6-7 show σI_{on} and $\sigma Log(I_{off})$ respectively. LER causes largest σI_{on} and $\sigma LogI_{off}$ of n-SOTB while LER and WFV together dominate that of p-SOTB. Fig. 8 shows fluctuated dependence of gate capacitance (C_g) on gate bias (V_g). LER, STV and WFV impact such σC_g-V_g relation differently, as illustrated in Fig.9. For n-SOTB LER dominates σC_g both at V_g =0.45V and 0.9V. For p-SOTB LER and WFV impact σC_g at V_g =-0.45V comparably while the high gate bias apparently reduces WFV-induced σC_g due to the screening effect of the inversion layer [6]. Considering that such kind of variable-γ SOTB MOSFET is attractive to application of logic circuit, we investigated its inverter delay-time (t_d) variability performance, as shown in Fig.10. As we can see, LER causes a variation of more than 10% both for t_{HL} and $t_{LH,}$ and beyond this WFV also introduces equally σt_{LH} compared to LER. STV causes least variation of t_{HL} and $t_{LH,}$.

Conclusions

In this study, we have investigated the influences of intrinsic parameter fluctuations in 20-nm-gate variable-γ SOTB MOSFETs. Our results show that side-gate bias impacts V_{th}-roll-off and σDIBL oppositely. LER is the most important fluctuation source both for n- and p-type variable-γ SOTB. Effect of WFV is starting to outstand in a scale of 20nm, especially in p-type. If STV follows the requirements of [4], it would not become a challenging problem compared to LER and WFV.

Acknowledgment

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References

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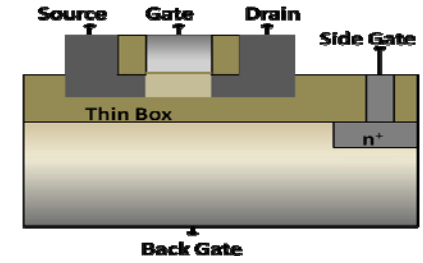


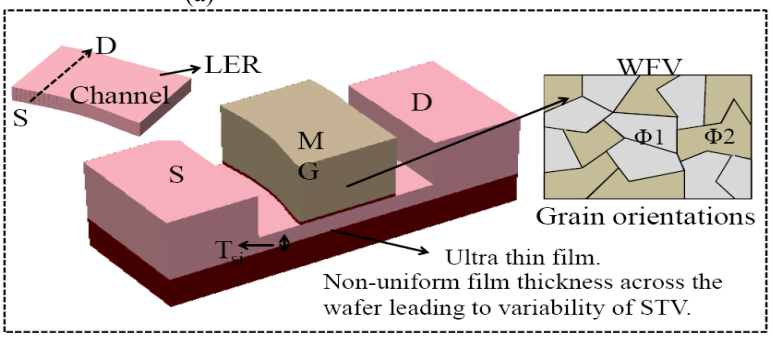
(a)

Material	Ori.	Prob	WF
TiN n-SOTB	<200>	60%	4.6 eV
	<111>	40%	4.4 eV
MoN p-SOTB	<110>	60%	5.0 eV
	<112>	40%	4.4 eV
Grain Size: Process depended. Here we assume 4nm both for TiN and MoN [9].			

(b)

PARAMETERS	VALUES
Nominal Gate Length (Lg)	20 nm
Channel Width (W)	30nm
Norminal Silicon Thickness (T_{si})	5.5nm
Box Thickness (T_{Box})	10nm
EOT	1.0 nm
S/D Doping Conc.	10^{20} cm^{-3}
Extension Doping Conc.	$5x10^{19}$ cm^{-3}
Channel Doping	intrinsic

(c)



(d)

Fig.1 Simulated structure: (a): Variable-γ n-SOTB. (b): Metal gate work-functions of different grain orientations. (c): Parameters used in the simulation. (d): Variability sources: (1) LER causes a variation of the effective channel length. (2) Different orientations have different WFs, and the effective WF is calculated as: $\Phi_{eff}=\Sigma\Phi_i P_i$. ($\Phi_i$ donates the WF, and P_i is the probability corresponding to Φ_i, as shown in (b)) (3) Non-uniform thickness of ultra-thin-film, used to control SCEs, leads to the variability of STV.

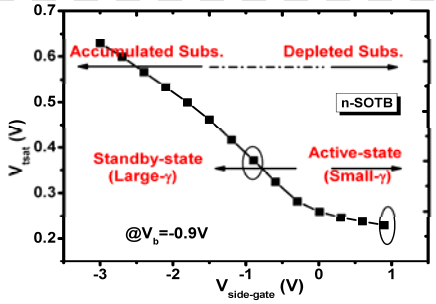


Fig.2 The side-gate bias tuning effect on γ of n-SOTB. Circled two points donate the selected work states (standby/active state) in this work.

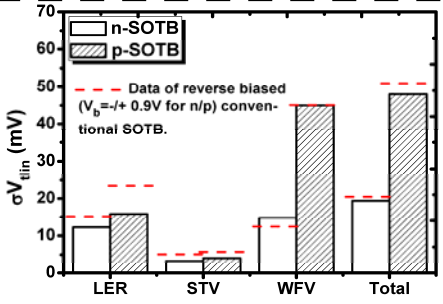


Fig.3 $|V_{tlin}|$ fluctuation for n- and p-type variable-γ SOTB MOSFETs. The dashed lines indicate values of conventional SOTB MOSFETs.

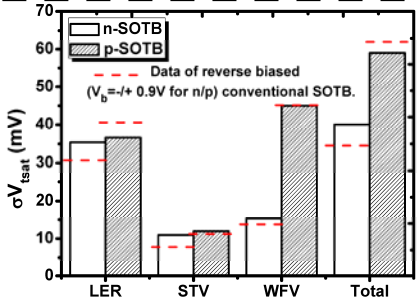


Fig.4 $|V_{tsat}|$ fluctuation for n- and p-type variable-γ SOTB MOSFETs. The dashed lines indicate values of conventional SOTB MOSFETs.

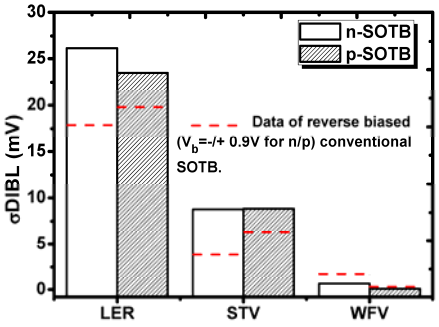


Fig.5 DIBL fluctuation for variable-γ n- and p- SOTB MOSFETs.

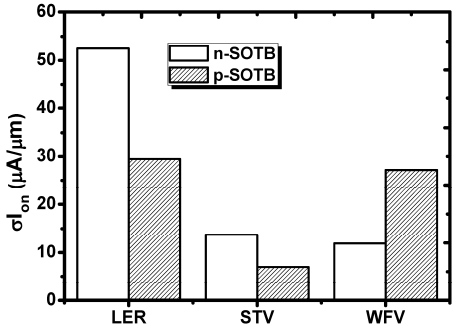


Fig.6 $|I_{on}|$ fluctuation for variable-γ n- and p- SOTB MOSFETs.

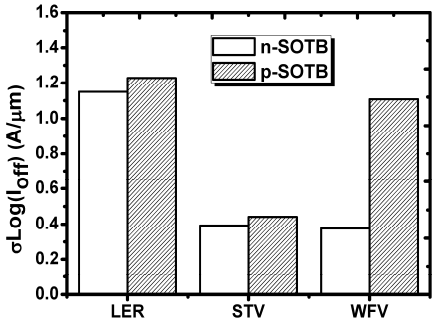


Fig.7 $|I_{off}|$ fluctuation for variable-γ n- and p- SOTB MOSFETs.

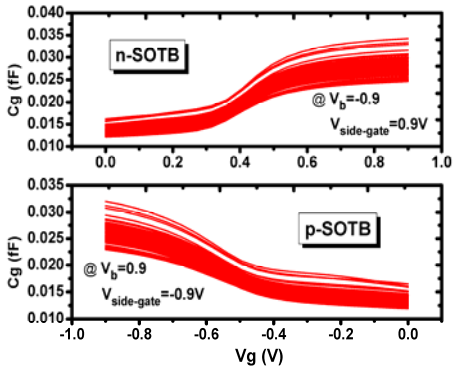


Fig.8 Disturbed dependence of C_g on V_g for variable-γ n- and p- SOTB MOSFETs.

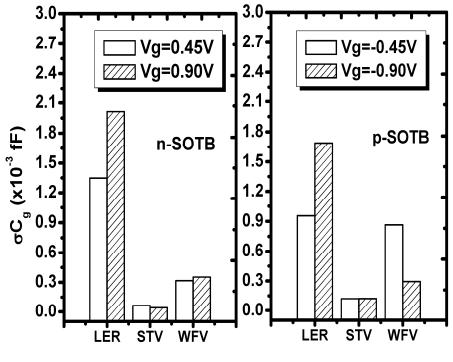


Fig.9 C_g fluctuation for variable-γ n- and p- SOTB MOSFETs under different V_g

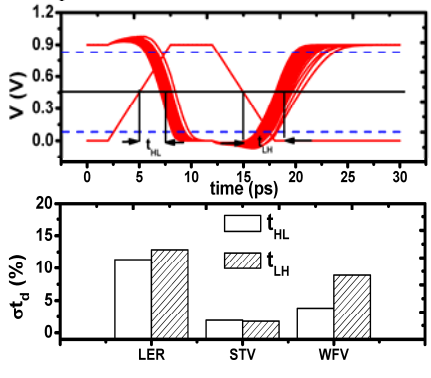


Fig.10 Inverter delay fluctuation for variable-γ n- and p- SOTB MOSFETs.