Extended Abstracts of the 2010 International Conference on Solid State Devices and Materials, Tokyo, 2010, pp1012-1013

Universal Relationship between Settling Time of Floating-Body SOI MOSFETs and the Substrate Current in their Body-Tied Counterparts

A. Toda[1], K. Ohyama[1], N. Higashiguchi[1], D. Hori[1], M. Miyake[1], S. Amakawa[1], J. Ida[2], and M. Miura-Mattausch[1]

[1]Hiroshima University
1–3–1 Kagamiyama, Higashi-Hiroshima 739–8530, Japan
[2]Kanazawa Institute of Technology
7–1 Ohgigaoka, Nonoichi, Ishikawa 921–8501, Japan

1. Motivation

Transient effects in floating-body SOI MOSFETs [1]–[3] present a big challenge to circuit designers. While there have been great advances in circuit design with SOI MOSFETs showing hysteretic behavior (e.g. [3], [4]), the subject remains a challenge because of the ever decreasing margin for design error and limited predictive power of circuit simulation currently available. Accurate modeling of the floating-body effects is essential for predictive SOI circuit simulation. DC floating-body effects have been modeled with reasonable success [5]. From a modeling standpoint, history effects in SOI MOSFETs are similar to non-quasistatic (NQS) effects in bulk MOSFETs and can be treated in essentially the same way [6]. An important step toward accurate modeling of history effects is to characterize the time constants involved in carrier accumulation in the floating body and model them. In this paper, we report on a device-size-independent universal relationship between the measured response time T_{d} of floating-body devices and the substrate current I_{sub} in body-tied devices.

2. Measurement of transients

All the devices we measured have the silicon film thickness of 40 nm, the gate oxide thickness of 2.5 nm, and the buried oxide thickness of 150 nm. Each device has a body terminal, through which I_{sub} can be measured. I_{d}-V_{d} characteristics of a device in the floating-body and body-tied conditions are shown in Fig. 1. The floating-body effect is suppressed when the body is tied to the ground.

The measurement setups for observing the transient response of an SOI MOSFET to an input voltage pulse are shown in Fig. 1. The input waveform is generated by an Agilent 81104A pulse generator and is applied to either the gate or the drain. The drain current I_{d} is measured by monitoring the voltage drop across the load resistor R_{L} with an HP 54845A oscilloscope. The dc bias is supplied by an Agilent 4156C semiconductor parameter analyzer.

When an input pulse with a steep ramp is applied to the gate of a floating-body device, I_{d} responds and reaches a steady state with some delay, T_{d}, as shown in Fig. 3(a). T_{d} depends very much on V_{d}. However, when the body of the device is tied to the ground, T_{d} is negligible and does not depend on V_{d} [Fig. 3(b)]. The transient responses of I_{d} to a pulse applied

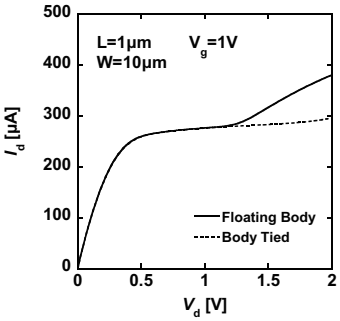

Fig. 1. Measured I_{d}-V_{d} characteristics of an SOI MOSFET. The body electrode was either left open (floating-body) or grounded (body-tied).

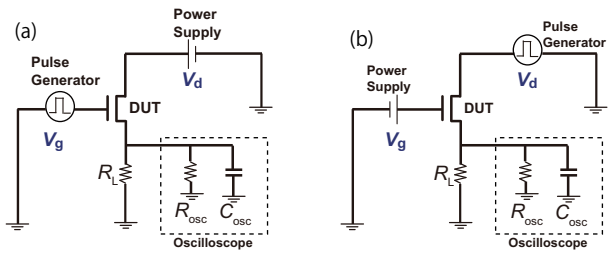

Fig. 2. Measurement setups for applying a pulse to the gate or the drain. I_{d} is monitored by using an oscilloscope. $R_{\mathrm{L}} = 50\,\Omega$, $R_{\mathrm{osc}} = 1\,\mathrm{M}\Omega$, $C_{\mathrm{osc}} = 12\,\mathrm{pF}$. (a) Pulsed-$V_{\mathrm{g}}$ measurement. (b) Pulsed-V_{d} measurement.

to the drain are shown in Fig. 4. As expected, pulse-height-dependent transient effects are observed in the case of the floating-body devices. Devices with other values of W and L showed similar results to Figs. 3 and 4.

3. Floating-body effect and body-tied substrate current

When T_{d} from the pulsed-V_{g} measurements are plotted against I_{sub} of the corresponding body-tied devices by making use of Fig. 5, the points lie on a nearly straight line independently of W and L, as shown in Fig. 6. Almost the same results are found from the pulsed-V_{d} measurements (Fig. 7).

The size-independent relationship between the floating-body T_{d} and the body-tied I_{sub} could be explained by considering an equivalent circuit shown in Fig. 8. In this model, the holes generated by impact ionization charge up the source-body junction and accumulate in the body. Then, the source-body voltage rises with $V_{\mathrm{sb}}(t) =$

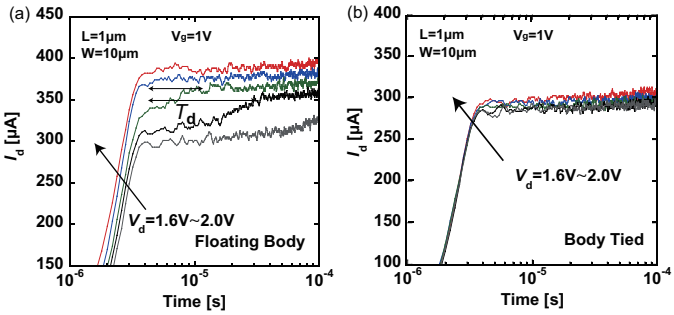

Fig. 3. Transient responses of I_{d} to a voltage pulse applied to the gate under different values of V_{d}. The pulse height is 1 V. I_{d} reaches a steady state after T_{d}. The rise time of the input pulse is 4 μs and the pulse width is long enough (200 ms) for reaching a steady state corresponding to Fig. 1. (a) Floating body. (b) Body tied.

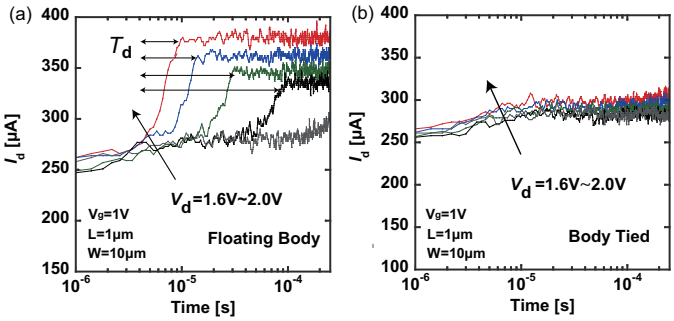

Fig. 4. Transient responses of I_{d} to a voltage pulse applied to the drain. The pulse heights are from 1.6 V to 2 V. (a) Floating body. (b) Body tied.

$R_{\mathrm{junc}} I_{\mathrm{sub}} \{1 - \exp[-t/(R_{\mathrm{junc}} C_{\mathrm{junc}})]\}$. Since $C_{\mathrm{junc}} \propto W$ and $R_{\mathrm{junc}} \propto 1/W$, and both C_{junc} and R_{junc} are independent of L, $T_{\mathrm{d}} \propto R_{\mathrm{junc}} C_{\mathrm{junc}}$ is independent of W and L.

4. Conclusion

We demonstrated a device-size-independent universal relationship between the settling time T_{d} of floating-body SOI MOSFETs in response to an input pulse and the substrate current I_{sub} in their body-tied counterparts. Such a universal relationship would allow one to accurately model SOI history effects using the technique for modeling non-quasistatic effects in bulk MOSFETs [6].

References

[1] J. Gautier, K. A. Jenkins, and J. Y.-C. Sun, IEDM Technical Digest, pp. 623–626, 1995

[2] S. Okhonin, M. Nagoga, J.-M. Sallese, P. Fazan, O. Faynot, J. Pontcharra, S. Cristoloveanu, H. van Meer, and K. De Meyer, Solid-State Electron., vol. 46, no. 11, pp. 1709–1713, 2002.

[3] V. Liot, P. Flatresse, J. M. Fournier, and M. Belleville, Solid-State Electron., vol. 49, pp. 1466–1476, 2005.

[4] G. G. Shahidi, F. Assaderaghi, and D. Antoniadis, "SOI technology and circuits," In A. Chandrakasan, W. J. Bowhill, and F. Fox, editors, *Design of High-Performance Microprocessor Circuits*, chap. 5, pp. 80–97, IEEE Press, 2001.

[5] T. Murakami, M. Ando, N. Sadachika, T. Yoshida, and M. Miura-Mattausch, Jpn. J. Appl. Phys., vol. 47, no. 4, pp. 2556–2559, April 2008.

[6] D. Navarro, Y. Takeda, M. Miyake, N. Nakayama, K. Machida, T. Ezaki, H. J. Mattausch, and M. Miura-Mattausch, IEEE Trans. Electron Devices, vol. 53, no. 9, pp. 2025–2034, September 2006.

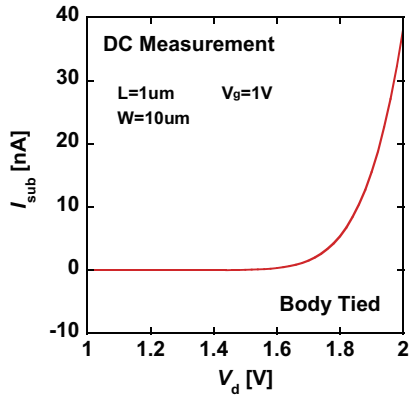

Fig. 5. Measured I_{sub}-V_{d} characteristics of an SOI MOSFET under the body-tied condition.

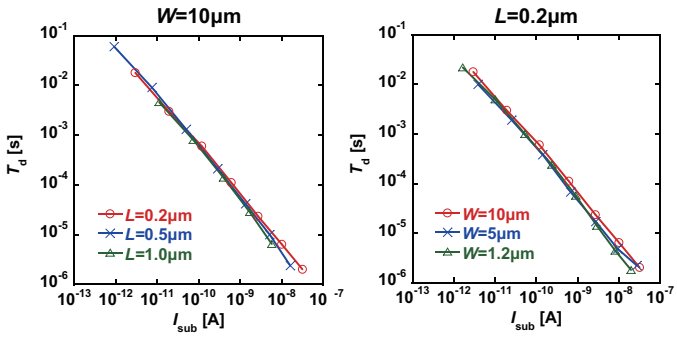

Fig. 6. Relationship between the T_{d} of floating-body devices and the I_{sub} of body-tied devices when a pulse is applied to the gate (Fig. 3).

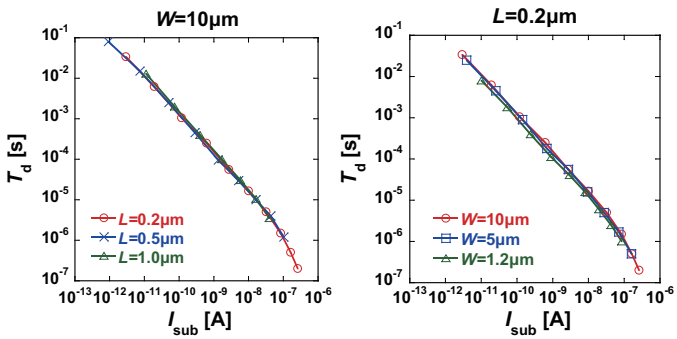

Fig. 7. Relationship between the T_{d} of floating-body devices and the I_{sub} of body-tied devices when a pulse is applied to the drain (Fig. 4).

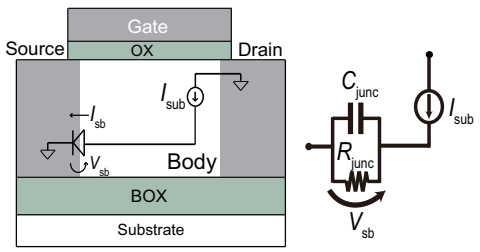

Fig. 8. A possible equivalent circuit representation.