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I_{on}-I_{off} performance analysis of FDSOI MOSFETs with low processing temperature

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Abstract

This work demonstrates that Fully-Depleted Silicon On Insulator (FDSOI) transistors processed at low temperature (overall process temperature kept below 600°C) exhibit no strong degradation of the off current as compared to their conventional Rapid Thermal Processing (RTP) counterparts. It is shown that tunnelling leakage is not the dominant mechanism of the leakage current and that the more abrupt junction achieved by Solid Phase Epitaxial Regrowth (SPER) is not problematic in terms of leakage current . Guidelines to achieve low access resistance within such a process are provided.

Introduction

Low temperature (LT) FDSOI processing -*i.e.* overall fabrication process temperature (T) below 600°C- arouses interest to alleviate gate stack challenges in terms of EOT [1], work function control and to obtain shallow junctions [2]. Furthermore, it is an asset in the perspective of 3D monolithic integration as it preserves the integrity of the bottom layer [1]. It has been previously observed that SPER leads to small access resistance, compatible with high performance FDSOI devices [1]. In this work, we show that the off current shows no strong degradation in the SPER devices compared to conventional RTP devices. A temperature analysis of the off-state current is performed in order to identify the dominant leakage mechanism.

Device fabrication

P and N type FDSOI transistors with 25 nm thick SOI film, 3 nm HfO_2 and TiN/Poly-Si gate stack were fabricated with a process where the fabrication T was kept below 600°C. The process is summarized in Fig.1. Special attention was paid to use LT oxide and nitride (for hardmask and spacers, respectively). The most challenging LT part *i.e.* dopant activation was realized thanks to the use of SPER. The SPER process is based on the LT recrystallization (occurring around 600°C) of pre-amorphized Si and results in a metastable electrical activation of the dopants above the solid solubility limit [3]. Reference devices with the conventional RTP activation were used for comparison.

Results and discussion

Ioff control

SPER activation around 600°C has proven to be efficient from an on-current point of view but it also leads to an increase of the off-current [4-8]. The low thermal budget is indeed insufficient to heal the end-of-range defects which are located just beyond the amorphized layer [5-8]. The residual defects intensify SRH recombination and trap assisted tunnelling (TAT). Additionally, the abrupt doping profile obtained thanks to the diffusionless activation mechanism may increase tunnelling. Fig.2 compares I_{on}-I_{off} values of the reference devices and SPER PFETs. It is observed that, with a FDSOI process, SPER devices can match the performance of their high T counterparts. Fig.3 displays the I_d-V_g characteristics with SPER and RTP in linear and saturation regime respectively. A slight current increase in accumulation for both N and P-type devices is observed in the saturation regime. Fig.4 shows the evolution of I_{dmin}, *i.e.* the minimum current reached in saturation: on average, SPER leads to a 1.5 decades increase of I_{dmin}. The I_d-V_g curves with V_d ramping up from 0.2V to 1.2 V are shown in Fig.5. It is observed that, with increasing V_d, Gate Induced Drain Leakage (GIDL) tends to occur at lower V_g. GIDL current can be caused by either trap induced leakage or tunnelling leakage. To investigate the dominant GIDL mechanisms, the I_d-V_g characteristics were studied, both in linear saturation regime, as a function of temperature. The corresponding plots are shown in Figs. 5 and 6 for N and PFET respectively. To determine whether tunnelling is the dominant mechanism of the leakage, $\log[I_d/(|V_{dg}|-1.2)^2]$ is plotted as a function of $1/(|V_{dg}|-1.2)$ (Figs. 7 and 8). A linear behaviour of this characteristic is the hallmark of tunnelling [9]. We observe that for RTP devices, both for N and P-type FETs, a linear behaviour is obtained at high $|V_g|$, indicating that tunnelling leakage is dominant under these biases [9]. At low $|V_g|$, the curves exhibit a plateau, whose length decreases with T, showing that defects assisted current is then the main mechanism involved. However the $\log[I_d/(|V_{dg}|-1.2)^2]$ curves of SPER devices at 300K do not show a linear behavior neither at low nor at high $|V_g|$, which indicates that tunnelling leakage is not the dominant leakage mechanism.

On current optimization

SPER is a diffusionless activation technique and therefore allows achieving ultra-shallow junctions. However, it is reported that dopants outside the amorphized region are not activated or that their dose is too small to fit the value targeted for extensions [5]. Using SPER in SOI requires accurate process tuning. Indeed, amorphization of the whole film suppresses the crystalline seed required for regrowth. As shown in Fig. 9, lateral recrystallization is unable to promote S/D regrowth. In Fig.10, the sheet resistance R_{sheet} of As doped (3keV through 3nm SiO_2) Si film is plotted as a function of Si thickness (T_{Si}) for several doses. R_{sheet} follows the theoretical $1/T_{Si}$ law up to a critical thickness (dependent on the dose) for which the film is fully amorphized during implantation, leading to a dramatic increase of R_{sheet}. From these data and atomistic simulations providing amorphization thickness [10], we can deduce that the minimum silicon thickness required for efficient recrystallization is around 1nm.

Conclusion

The off-state performance of SPER and RTP FDSOI transistors are compared. It is shown that for PFETs the same I_{on}-I_{off} trade-off could be reached. I_{dmin} is slightly larger in the case of SPER compared to RTP. The increase is not attributed to tunnelling leakage but to implantation defects. This offers the perspective of improving the leakage performance by implantation engineering in SPER. Also, it is shown that lateral recrystallization is insufficient to induce regrowth in the extension region. However, a 1 nm thick crystalline seed is shown to be sufficient for the extension vertical regrowth.

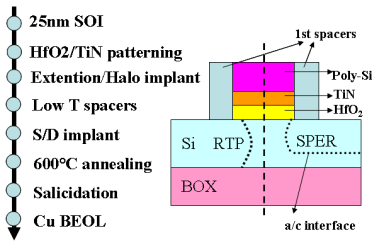

Fig.1: Left – Process flow. Right – Schematics of the devices showing the need to target different implantation depending on process temperature.

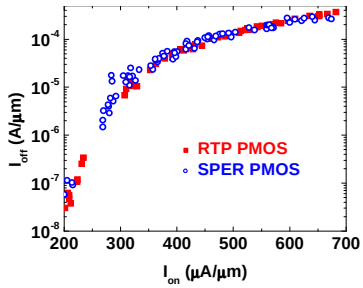

Fig.2: I_{on}-I_{off} of P type FDSOI SPER and RTP reference devices showing that SPER can match the high T performance.

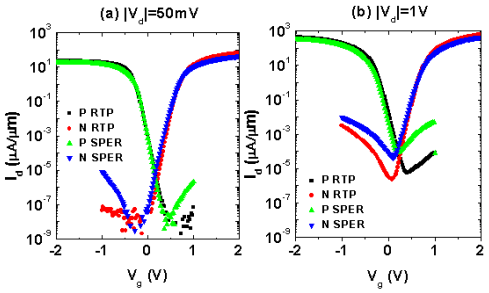

Fig.3: I_d-V_g in the linear (a) and the saturation (b) regime for N and P SPER and RTP FDSOI FETs with Lg=150nm.

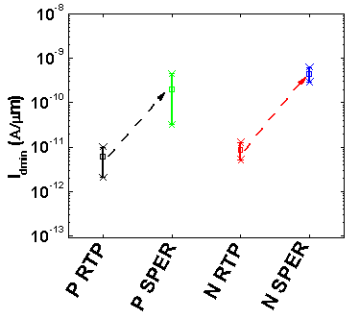

Fig.4: Statistical I_{dmin} of N and P MOS at room temperature. I_{dmin} is the smallest value achieved in saturation.

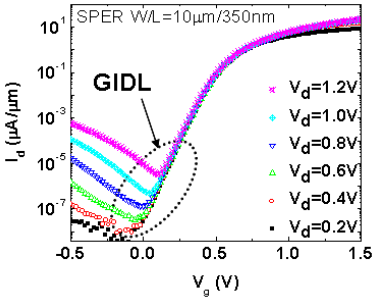

Fig.5: I_d-V_g of a SPER NFET at different V_d, at 300K..As V_d increases, GIDL tends to occur at lower V_g.

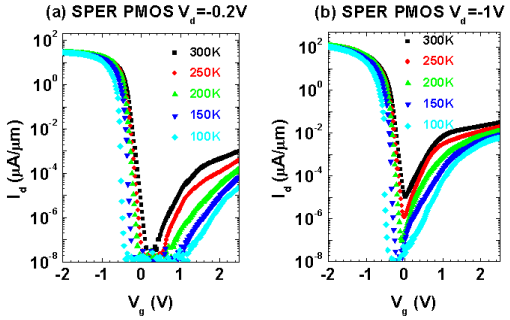

Fig.6: I_d-V_g of a SPER PFET as a function of T at V_d=-0.2V (a) and V_d=-1V (b).

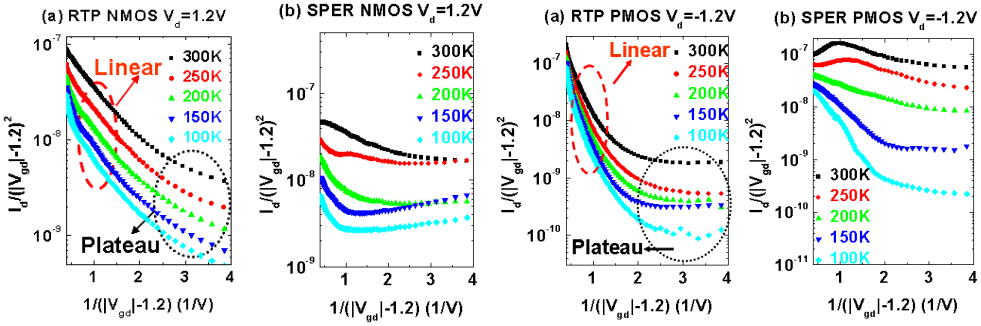

Fig.7: $\log[I_d/(|V_{dg}|-1.2)^2]$ vs. $1/(|V_{dg}|-1.2)$ of RTP (a) and SPER (b) NMOS. In the linear and saturation regions, the current is dominant by tunnelling and defects induced leakage respectively.

Fig.8: $\log[I_d/(|V_{dg}|-1.2)^2]$ vs. $1/(|V_{dg}|-1.2)$ of RTP (a) and SPER (b) PMOS. In the linear and saturation regions, the current is dominant by tunnelling and defects induced leakage respectively.

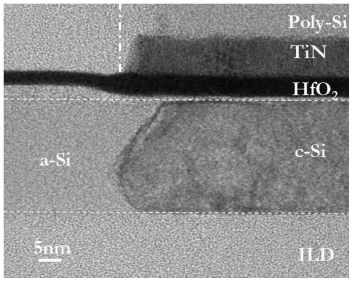

Fig.9: TEM X-section of a FDSOI FET after amorphizing implantation and 600°C annealing. No lateral recrystallization is observed outside the gate.

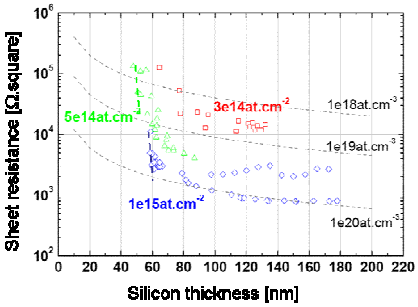

Fig.10: Sheet resistance as a function of Silicon thickness of a As implanted (3keV through 3nm screen oxide) SOI film.

Acknowledgments

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