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Cost Efficient Novel High Performance Analog Devices Integrated with Advanced HKMG Scheme for 28nm CMOS Technology and Beyond

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Introduction: Integrating high-performance analog and digital devices in low-power CMOS provides significant advantages for system-on-chip (SOC) designs. Technology scaling has provided benefits for analog design such as improved mismatch with Tox reduction. However, transistor self-gain and 1/f noise deteriorate as the channel doping concentration increases; it also limits the improvement in mismatch from Tox scaling. In poly-SiON gate technologies, ion implant (I/I) optimization, skipped halo I/I, shallow halo angles with additional masks, and parallel halo I/I have been demonstrated to improve analog transistors [1-4]. In HKMG technologies, there has been concern that interface traps could degrade analog behavior. However, analog performance comparable to that of SiON has been recently been demonstrated in a HKMG technology [5]. In this paper, further analog transistor optimization of this HKMG technology is presented.

High Performance Analog (HPA): Novel HPA devices in a gate first based HKMG scheme with innovative halo engineering have been successfully demonstrated to produce superior analog and digital performance for low power applications such as mobile phones without additional cost [5]. These HPA devices are "free" devices and can easily be integrated with either HKMG gate first or replacement metal gate (RMG) processes. The digital and analog devices are built simultaneously in a further improved process with no extra mask, no extra litho, and no extra process step. For the first time, a comprehensive study of the analog and digital characteristics of these HPA devices has been carried out. In addition to analog properties such as output voltage gain, Gm, Gds, Gm/Id, mismatch behavior, flicker noise, linearity, DC performance (e.g. Ion-Ioff, Ioff-Vtsat, DIBL, Cjswg) as well as reliability have been evaluated. Figs. 1(a) - (d) show schematics of transistors with options of (a) quad halo I/I, (b) dual vertical (to PC) halo I/I, (c) dual horizontal halo I/I, and (d) no halo I/I. Option (c) is developed in this paper with (a) as analog control.

Digital Performance: In comparison with analog controls, Ion-Ioff of HPA 1μm x 3*Lnom devices shows ~11% and ~14% improvement for nFETs (Fig. 2a) and pFETs (Fig. 2b) respectively. The sub-threshold characteristic (Ioff-Vtsat) of HPA devices also improve as shown in both Figs. 3a (nFETs) and 3b (pFETs). As expected, the sidewall capacitance (Cjswg) of HPA devices shows significant reduction compared to analog controls for both RVT and LVT n/pFETs (Figs. 4a, b). This combined result indicates a positive impact on performance without significant degradation of short channel effects due to the relatively relaxed length of the analog devices.

Analog Performance: For 1μm x 1μm nFETs, the iGain of the HPA devices is significantly improved (Fig. 5a) over analog controls, showing the best results among reported SiON and HKMG values [5,6]. The transconductance of the HPA devices at the operation point shows a noticeable improvement (Fig. 5b) while the Gds reflects a clear reduction (Fig. 6a). This result is consistent with the DIBL reduction of the HPA devices with channel length >3*Lnom over analog controls in Fig. 6b. DIBL reduction is likely due to drain side barrier height reduction with reduced halo in the channel. Similar trends of iGain, Gm and Gds are seen for pFETs (not shown). Gm/Id versus Lgate of HPA devices improved over controls for nFET and pFET (Figs. 7a, b). Gm-Id and sqrt(Gm/G3)-Id of 1μm x 3*Lnom nFETs revealed enhanced Gm at a given Id and clearly better linearity (Figs. 7c,d). An example of the HPA pFETs low frequency 1/f noise spectrum is shown with controls in Fig. 8. The inset shows details at low frequency. Lack of halo in the channel has lowered HPA normalized flicker noise because of less halo induced trapping for both n- and p-type. While it is expected the HKMG induced number and mobility fluctuation can be further optimized, these values are comparable to or lower than SiON analog devices at low frequency [6]. In addition, the HPA devices show clear Vt mismatch (MM) advantage (Figs. 9a, b). The AVT values can reach 1.6-1.7, the lowest values ever reported [5, 6]. For the first time, length dependence of DIBL MM of HPA devices are evaluated and show better than control with an interesting U-shape. This shape may be attributed to the lower DIBL and a more uniform edge-center profile for the channel doping. Since the HPA halo I/I was parallel to PC, DIBL MM is more sensitive on the edge than for the 'well FET' controls [7].

Reliability: Hot Carrier Injection (HCI) shows similar or improved Id shift and Vtsat shift at a given stress time on the HPA devices compared to analog controls.

Conclusion: The reported HKMG HPA devices have demonstrated superior self-gain, matching, linearity and flicker noise, digital performance and reliability. Some results are the best reported for both HKMG and poly-SiON technologies.

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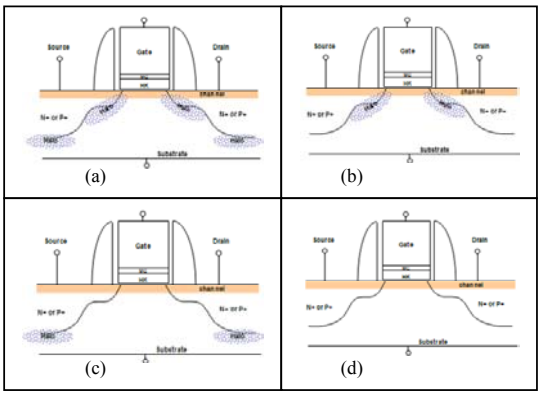

Fig. 1. Schematics of transistors with options of (a) quad halo I/I, (b) dual vertical (to PC) halo I/I, (c) dual horizontal halo I/I, (d) no halo I/I ; HPA devices are (c) and (d), while (a) and (b) are analog controls.

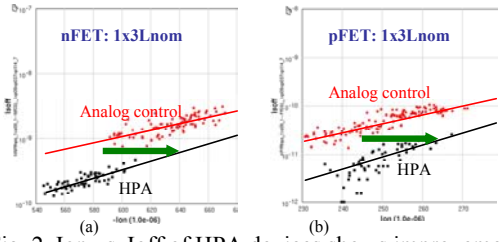

Fig. 2. Ion vs. Ioff of HPA devices shows improvement over control on (a) nFETs (b) pFETs.

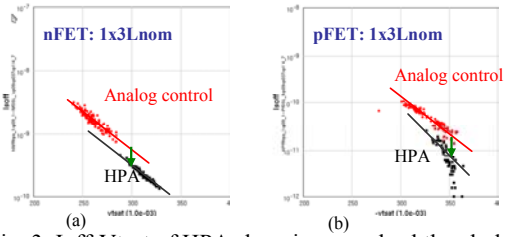

Fig. 3. Ioff-Vtsat of HPA show improved subthreshold characteristics for both (a) nFETs (b) pFETs.

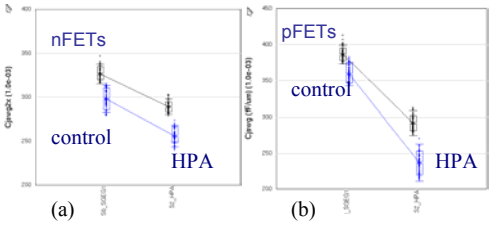

Fig.4. sidewall capacitance Cjswg of HPA devices show significant reduction for both (a) nFETs (b) pFETs compared to control.

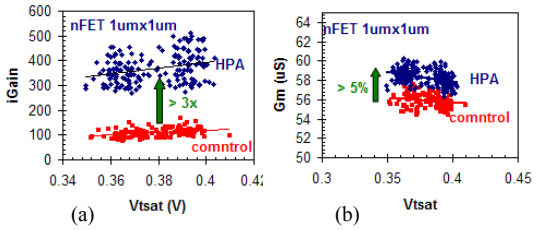

Fig. 5. (1) iGain of HPA devices increases significantly compared to control on nFETs, (b) Gm shows improvement too. Similar improvement was seen on pFETs (not shown here).

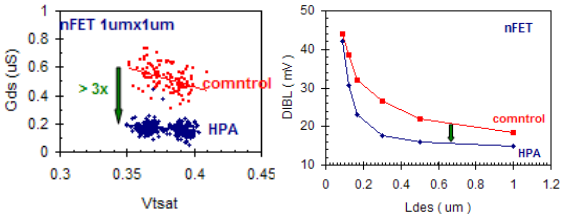

Fig. 6. HPA devices show reduction on nFETs with (a) Gds (b) DIBL (>3Lnom) compared to control; similar improvement on pFETs (not shown here)

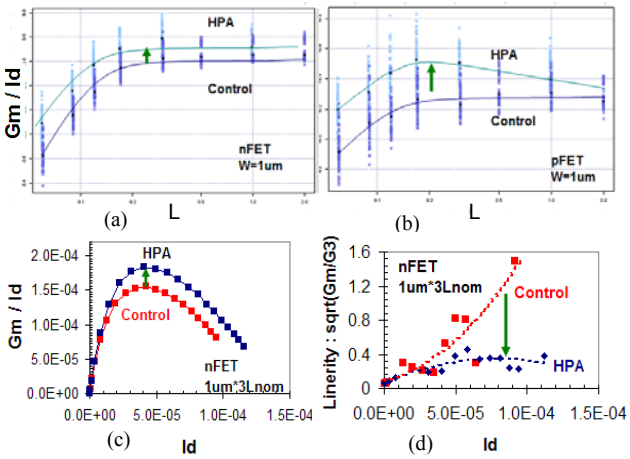

Fig.7. Gm/Id (vs L) of HPA devices in comparison with analog control shows improvement for (a) nFET (b) pFET. Example of nFETs 1x3Lnom (c) Gm vs. Id (d) sqrt(Gm/G3) vs. Id show clear improvement in term of transconductance at given drain current and linearity.

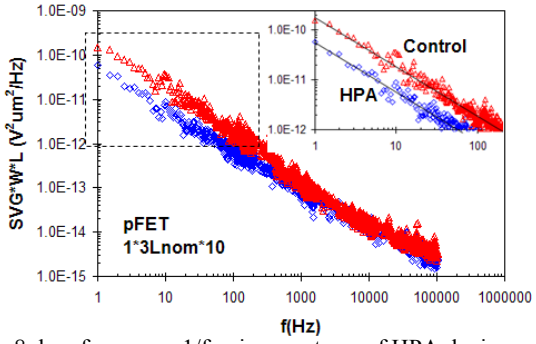

Fig.8. low frequency 1/f noise spectrum of HPA devices show reduction compared to analog control, example of pFET is shown here. The insets are flick noise zoom-in spectrum at low frequency. Similar improvement is seen on nFETs (not shown).

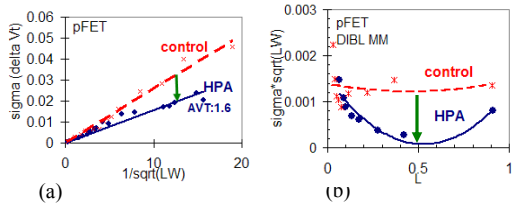

Fig.9. pFETs HPA Vt mismatch show (a) AVT reduction over control, while length dependence of (b) DIBL mismatch of HPA show reduction with an interesting U-shape trend with 2nd order polynomial fitting. Similar improvement is seen on nFETs (not shown).