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Experimental Study of PVD-TiN Gate with Poly-Si Capping and Its Application to 20 nm FinFET Fabrication

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1. Introduction

Recently, as one of the promising metal gate materials, PVD-TiN has actively been used in the undoped channel FinFET fabrication because its midgap work function offers a symmetrical threshold voltage (V_{th}) without channel doping [1-5]. However, the electrical characteristics of scaled PVD-TiN gate FinFETs including the V_{th} variability and mobility have not been investigated sufficiently.

In this paper, we present the detailed comparison of the V_{th} variations and mobilities of the fabricated n^+-poly-Si gate and PVD-TiN gate FinFETs with a (111)-oriented channel surface, and discuss the superiority of the PVD-TiN gate with n^+-poly-Si capping.

2. Device fabrication

Figure 1 shows the abbreviated device fabrication flow. Except the gate stack deposition and RTA steps, the devices were fabricated with the same process. Si-fin channels were fabricated by using the orientation-dependent wet etching on the (110) SOI wafers [1]. After the gate oxidation, a 100-nm-thick n^+-poly-Si layer was deposited as a gate material for type-A samples, and 20-nm-thick PVD-TiN & 100-nm-thick n^+-poly-Si layers were continuously deposited for type-B samples. After the ion implantation (I/I) and a 100-nm-thick CVD-SiO_2 layer deposition, RTA was performed at 900 ^oC for type-A and 830 ^oC for type-B devices with the same time of 2 s.

3. Experimental results and discussion

The SEM image of the fabricated n^+-poly-Si gate FinFET is shown in Fig. 2. It is clear that 20-nm gate (L_g) is successfully fabricated. The cross-sectional STEM images of the fabricated FinFETs are shown in Figs. 3. Note that ideal rectangular cross-section Si-fins are formed uniformly thanks to the orientation-dependent wet etching.

Figures 4(a) and 4(b) show the typical I_d-V_g characteristics of the fabricated FinFETs with L_g = 20 and 40 nm, respectively. Note that L_g = 20 nm FinFETs show normal transistor characteristics although the S-slope and DIBL are slightly larger than those of L_g = 40 nm devices. Moreover, it is clear that symmetrical I_d-V_g curves are obtained by introducing PVD-TiN gate instead of the n^+-poly-Si gate thanks to the midgap work function of PVD-TiN gate. Figure 5 summarizes the measured V_{th} and S-slope at V_d = 0.05 V. It can be seen that V_{th} and S-slope keep almost constant values at L_g > 50 nm, indicating a good short-channel effects (SCEs) immunity. To suppress the SCEs at L_g < 50 nm, a thin gate sidewall spacer is required before source-drain (SD) extension I/I process [6], which is under development.

Figure 6 shows the device dimension variations including Si-fin thickness (T_{Si}) and L_g by SEM. Average $\langle T_{Si} \rangle$ & $\langle L_g \rangle$ are 23.4 and 100.8 nm, and the small σT_{Si} = 3.7 & σL_g = 3.6 nm are obtained by optimizing fabrication process. The measured I_d-V_g characteristics of the fabricated n-channel FinFETs with the same $\langle L_g \rangle$ = 100.8 nm are shown in Fig. 7(a), and the corresponded statistical V_{th} variations are shown in Fig. 7(b). It is clear that almost the same σV_{th} is obtained in the cases of n^+-poly-Si gate and PVD-TiN gate. Such result is further confirmed in the case of L_g = 150 nm as shown in Fig. 8. Thus, it is concluded that PVD-TiN gate enables to set a symmetrical V_{th} for undoped channel FinFET CMOS without increasing V_{th} variations.

In order to evaluate carrier mobility, split C-V of the fabricated multi-FinFETs was measured as shown in Fig. 9. The measured mobility data are shown in Fig. 10. Note that the measured mobility data of the n^+-poly-Si gate and PVD-TiN gate show almost the same values, and the electron mobility data show good agreement with the universal mobility curve of the (111) bulk MOSFETs [7, 8], due to the damage-free Si-fin channels by the wet process. Furthermore, it can be confirmed that n^+-poly-Si capping on 20-nm-thick PVD-TiN layer is very effective to improve mobility both for electrons and holes compared to the pure 50-nm-thick PVD-TiN gate without n^+-poly-Si capping. Such mobility improvement is possibly resulted from the retardation of PVD-TiN induced mechanical stress [9] by introducing a thin 20 nm PVD-TiN and a thick 100 nm n^+-poly-Si capping layer.

4. Conclusion

We have comparatively investigated the electrical characteristics including V_{th} variability and mobility by fabricating a series of n^+-poly-Si and PVD-TiN gate FinFETs, and demonstrated 20 nm L_g FinFETs. It was experimentally found that 20-nm PDV-TiN with n^+-poly-Si capping is very effective to set a symmetrical V_{th} for undoped FinFET CMOS without σV_{th} and mobility degradations compared to n^+-poly-Si gate FinFETs. The developed PVD-TiN gate technology is very useful for the scaled FinFET circuit fabrication.

Acknowledgements

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References

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- Thermal oxidation of (110)SOI
- Fin-patterning in the <112> direction
- Si-fin-fabrication by TMAH
- Gate oxidation at 850 °C
- Gate material deposition
  - A: n^+-poly-Si
  - B: PVD-TiN with n^+-poly-Si capping
- Extension I/I ($D = 1\times10^{14}$cm^{-2}, $\theta = 60°$)
- Gate sidewall formation
- SD electrode I/I ($D = 1.5\times10^{15}$cm^{-2})
- RTA (t =2s), 900°C for A, 830°C for B
- Metallization and PMA at 450°C for 30 min.

Fig. 1. Device fabrication process flow with different gate materials.

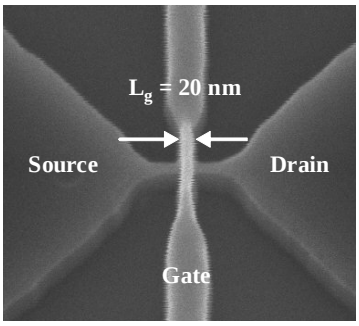


Fig. 2. SEM image of the fabricated n^+-poly-Si gate FinFET with L_g = 20 nm.

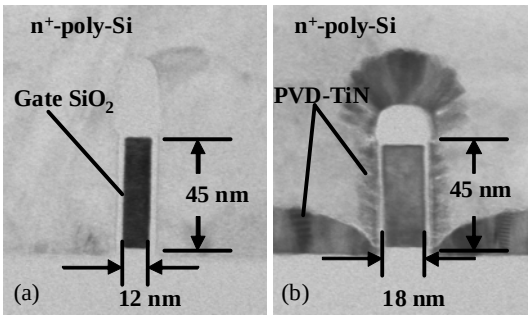
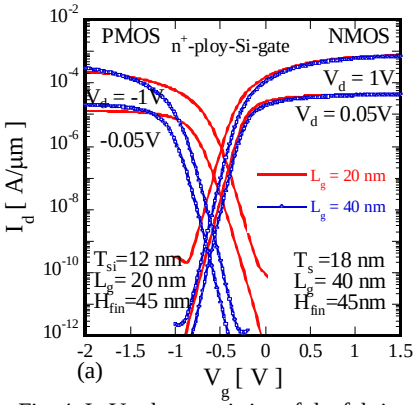


Fig. 3. Cross-sectional STEM images of the fabricated (a) n^+-poly-Si gate, and (b) PVD-TiN gate FinFETs.



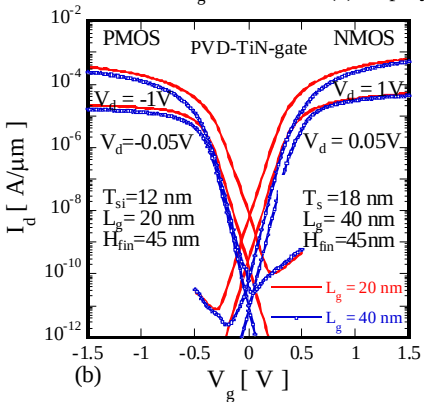


Fig. 4. I_d-V_g characteristics of the fabricated (a) n^+-poly-Si and (b) PVD-TiN gate FinFETs. Almost symmetrical I_d-V_g curve is obtained by introducing PVD-TiN gate.

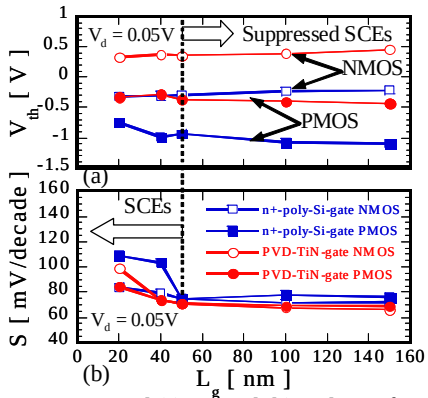
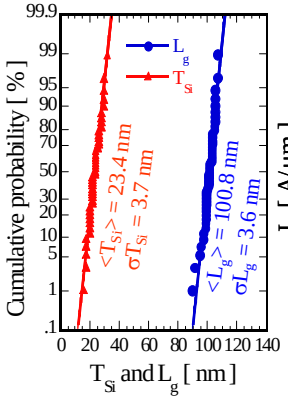
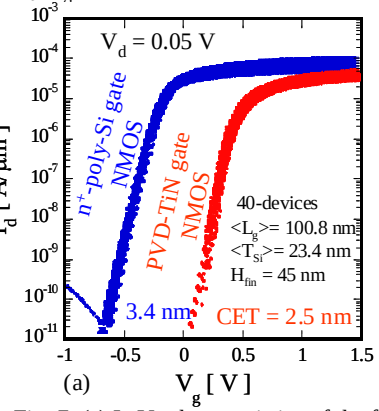


Fig. 5. Measured (a) V_{th} and (b) S-slope of the fabricated devices as a function of L_g.





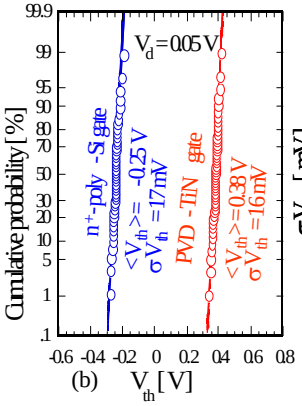


Fig. 6. Variations of T_{Si} and L_g measured by SEM.

Fig. 7. (a) I_d-V_g characteristics of the fabricated n-channel FinFETs with the same L_g = 100 nm, and (b) the corresponded statistical V_{th} variations.

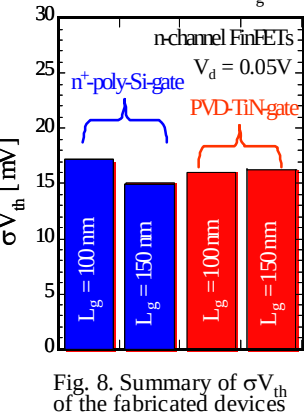
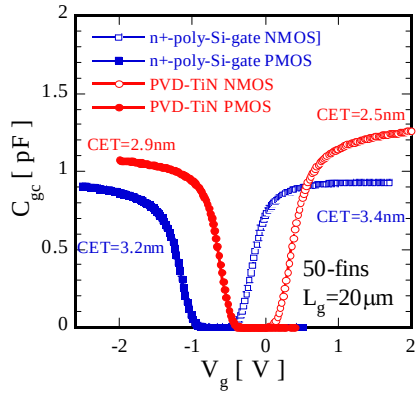
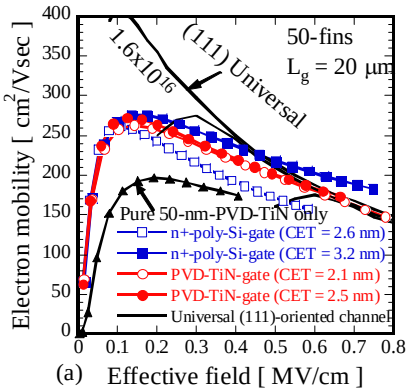


Fig. 8. Summary of σV_{th} of the fabricated devices with different L_g's of 100 and 150 nm.





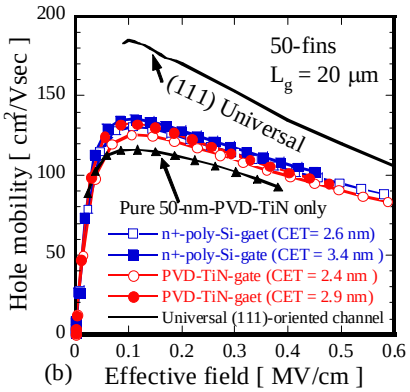


Fig. 9. C_{gc}-V_g characteristics of the fabricated multi-FinFETs with 50-fins and L_g = 20 μm.

Fig. 10. Comparison between measured (a) electron and (b) hole mobility data of the multi-FinFETs and universal mobility data of (111) bulk MOSFETs.