Experimental Study of PVD-TiN Gate with Poly-Si Capping and Its Application to 20 nm FinFET Fabrication

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C-7-1

1. Introduction

Recently, as one of the promising metal gate materials, PVD-TiN has actively been used in the undoped channel FinFET fabrication because its midgap work function offers a symmetrical threshold voltage ($V_{th}$) without channel doping [1-5]. However, the electrical characteristics of scaled PVD-TiN gate FinFETs including the $V_{th}$ variability and mobility have not been investigated sufficiently.

In this paper, we present the detailed comparison of the $V_{th}$ variations and mobilities of the fabricated n-poly-Si gate and PVD-TiN gate FinFETs with a (111)-oriented channel surface, and discuss the superiority of the PVD-TiN gate with n-poly-Si capping.

2. Device fabrication

Figure 1 shows the abbreviated device fabrication flow. Except the gate stack deposition and RTA steps, the devices were fabricated with the same process. Si-fin channels were fabricated by using the orientation-dependent wet etching on the (110) SOI wafers [1]. After the gate oxidation, a 100-nm-thick n-poly-Si layer was deposited as a gate material for type-A samples, and 20-nm-thick PVD-TiN & 100-nm-thick n-poly-Si layers were continuously deposited for type-B samples. After the ion implantation (I/I) and a 100-nm-thick CVD-SiO2 layer deposition, RTA was performed at 900°C for type-A and 830°C for type-B devices with the same time of 2 s.

3. Experimental results and discussion

The SEM image of the fabricated n-poly-Si gate FinFET is shown in Fig. 2. It is clear that 20-nm gate ($L_{g}$) is successfully fabricated. The cross-sectional STEM images of the fabricated FinFETs are shown in Figs. 3. Note that ideal rectangular cross-section Si-fins are formed uniformly thanks to the orientation-dependent wet etching.

Figures 4(a) and 4(b) show the typical $I_{d}-V_{g}$ characteristics of the fabricated FinFETs with $L_{g} = 20$ and 40 nm, respectively. Note that $L_{g} = 20$ nm FinFETs show normal transistor characteristics although the S-slope and DIBL are slightly larger than those of $L_{g} = 40$ nm devices. Moreover, it is clear that symmetrical $I_{d}-V_{g}$ curves are obtained by introducing PVD-TiN gate instead of the n-poly-Si gate thanks to the midgap work function of PVD-TiN gate. Figure 5 summarizes the measured $V_{th}$ and S-slope at $V_{g} = 0.05$ V. It can be seen that $V_{th}$ and S-slope keep almost constant values at $L_{g} > 50$ nm, indicating a good short-channel effects (SCEs) immunity. To suppress the SCEs at $L_{g} < 50$ nm, a thin gate sidewall spacer is required before source-drain (SD) extension I/I process [6], which is under development.

Figure 6 shows the device dimension variations including Si-fin thickness ($T_{Si}$) and $L_{g}$ by SEM. Average $<T_{Si}>$ & $<L_{g}>$ are 23.4 and 100.8 nm, and the small $\sigma_{T_{Si}} = 3.7$ & $\sigma_{L_{g}} = 3.6$ nm are obtained by optimizing fabrication process. The measured $I_{d}-V_{g}$ characteristics of the fabricated n-channel FinFETs with the same $<L_{g}> = 100.8$ nm are shown in Fig. 7(a), and the corresponded statistical $V_{th}$ variations are shown in Fig. 7(b). It is clear that almost the same $\sigma V_{th}$ is obtained in the cases of n-poly-Si gate and PVD-TiN gate. Such result is further confirmed in the case of $L_{g} = 150$ nm as shown in Fig. 8. Thus, it is concluded that PVD-TiN gate enables to set a symmetrical $V_{th}$ for undoped channel FinFET CMOS without increasing $V_{th}$ variations.

In order to evaluate carrier mobility, split C-V of the fabricated multi-FinFETs was measured as shown in Fig. 9. The measured mobility data are shown in Fig. 10. Note that the measured mobility data of the n-poly-Si gate and PVD-TiN gate show almost the same values, and the electron mobility data show good agreement with the universal mobility curve of the (111) bulk MOSFETs [7, 8], due to the damage-free Si-fin channels by the wet process. Furthermore, it can be confirmed that n-poly-Si capping on 20-nm-thick PVD-TiN layer is very effective to improve mobility both for electrons and holes compared to the pure 50-nm-thick PVD-TiN gate without n-poly-Si capping. Such mobility improvement is possibly resulted from the retardation of PVD-TiN induced mechanical stress [9] by introducing a thin 20 nm PVD-TiN and a thick 100 nm n-poly-Si capping layer.

4. Conclusion

We have comparatively investigated the electrical characteristics including $V_{th}$ variability and mobility by fabricating a series of n-poly-Si and PVD-TiN gate FinFETs, and demonstrated 20 nm $L_{g}$ FinFETs. It was experimentally found that 20-nm PDV-TiN with n-poly-Si capping is very effective to set a symmetrical $V_{th}$ for undoped FinFET CMOS without $\sigma V_{th}$ and mobility degradations compared to n-poly-Si gate FinFETs. The developed PVD-TiN gate technology is very useful for the scaled FinFET circuit fabrication.

Acknowledgements

This work was supported in part by the Development of Nanoelectronics Device Technology of NEDO Japan.

References
Fig. 6. Variations of TSi and Lg [nm].

Fig. 1. Device fabrication process flow with different gate materials.

Fig. 2. SEM image of the fabricated n+-poly-Si gate FinFET with Lg = 20 nm.

Fig. 9. Cgc-Vg characteristics of the fabricated multi-FinFETs and universal mobility data of (111) bulk MOSFETs.

Fig. 5. Measured (a) Vth and (b) S-slope of the fabricated devices as a function of Lg [nm].

Fig. 8. Summary of σVth of the fabricated devices with different Lg [μm] of 100 and 150 nm.

Fig. 7. (a) I-V characteristics of the fabricated n-channel FinFETs with the same Lg = 100 nm, and (b) the corresponding statistical Vth variations.

Fig. 10. Comparison between measured (a) electron and (b) hole mobility data of the multi-FinFETs and universal mobility data of (111) bulk MOSFETs.