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# High-k Metal Gate FinFET SRAM Cell Optimization Considering Variability due to NBTI/PBTI and Surface Orientation

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## Abstract

This paper analyzes the impact of intrinsic process variation and NBTI/PBTI induced time-dependent variations on the stability/variability of 6T high-k metal gate FinFET SRAM cells with various surface orientations. Due to quantum confinement, (110)-oriented pull-down devices with fin Line Edge Roughness (LER) show larger Vread,0 and Vtrip variations, thus degrading RSNM and its variability. (100)-oriented pull-up devices with fin LER show larger Vwrite,0 and Vtrip variations, hence degrade the variability of WSNM. The combined effects of intrinsic process variation and NBTI/PBTI induced variations have been examined to optimize the FinFET SRAM cells. Worst-case stress scenario for SNM stability/variability is analyzed. With both NBTI and PBTI in high-k metal gate FinFET SRAM, the RSNM suffers significant degradation as Vread,0 increases while Vtrip decreases simultaneously. Variability comparisons for FinFET SRAM cells with different gate stacks ($SiO_2$ and $SiO_2/HfO_2$) are also examined. Our study indicates that consideration of NBTI/PBTI induced temporal variation changes the optimal choice of FinFET SRAM cell surface orientations in term of μRSNM/σRSNM.

## Introduction

Multi-gate FinFETs are promising device candidates for post-22 nm CMOS technology generations due to their superior short channel effects, better subthreshold slope, and reduced random dopant fluctuation. The sidewall surface (conducting channel) orientation of FinFET devices can be easily changed by rotating the layout of the devices to improve electron and hole mobility [1]. Negative and Positive Bias Temperature Instabilities (NBTI (for PFET) and PBTI (for NFET)) have become major long-term reliability concerns as they weaken MOSFETs over time, thus resulting in temporal degradation in the stability of the SRAM cells [2-4]. FinFET devices with different surface orientations exhibit distinct threshold voltage variations resulting from intrinsic process variations and NBTI/PBTI induced temporal variations. Fig. 1(a) and (b) illustrate the 6T FinFET SRAM cells with (110)/(100) surface (conducting channel) orientations by rotating the FinFET devices. The layouts are based on scaled ground rules from 32 nm node according to ITRS projection. In this work, for the first time, the combined effects of short-term intrinsic process variability and long-term temporal variability (due to NBTI/PBTI) are considered for optimizing the FinFET device orientation combinations to improve the stability/variability of 6T high-k metal gate FinFET SRAM cells.

## Device Design and Simulation Methodology

In this work, 6T FinFET SRAM designed with 18nm ($L_g$) FinFET devices ($W_{fin}$=5nm, $H_{fin}$=15nm, channel doping=1e17cm$^{-3}$, $V_{dd}$=1V, gate stacks: $SiO_2$(0.6nm)/$HfO_2$(2.5nm) or $SiO_2$(1nm)) are analyzed using mixed-mode simulation [5]. The quantum-confinement effect is calibrated with exact solution of Schrödinger's equation to accurately consider the threshold voltage sensitivity to process variation for (100)/(110) N/PFETs. Reaction-Diffusion model [6] is used to calibrate the threshold voltage drift due to NBTI/PBTI [7, 8]. To assess the dominant process variation source, fin LER [9], the line edge patterns have been derived using Fourier synthesis [10], and 3D mixed-mode Monte Carlo simulations with 200 samples were then performed for each case.

## 6T FinFET SRAM Cells with (110)/(100) Surface Orientations

Pull-up (PU), pull-down (PD) and pass-gate (PG) transistors with (110) and (100) orientations can be combined for 8 types of 6T FinFET SRAM cells. Fig. 2 shows the RSNM (Read Static Noise Margin) and Vread,0/Vtrip (defined in Fig. 4(a) inset) comparisons among the 8 types of cells. FinFET SRAM cells with (110) PG show lower Vread,0 and higher RSNM than that with (100) PG. (PU,PD,PG)=(110,100,110) and (100,100,110) show higher RSNM than the standard SRAM cell with all (110) devices. Fig. 3 shows the WSNM (Write Static Noise Margin) and Vwrite,0/Vtrip (defined in Fig. 4(b) inset) comparisons. (100) PG with stronger strength shows lower Vwrite,0 and larger WSNM.

*A. Short-Term Stability/Variability due to Process Variation*

Fig. 4 shows degraded Read/Write stability of 6T FinFET SRAM cell due to LER. Fig. 5(a) shows the normalized σRSNM and μRSNM/σRSNM comparisons among the 3 types of FinFET SRAM cells which have higher RSNM. SRAM cell with orientation (PU,PD,PG) = (100,100,110) shows larger σRSNM than the (110,100,110) one. Because (100) PU device with stronger quantum confinement exhibits larger threshold voltage variation due to fin LER than the (110) PU device, the (100,100,110) SRAM cell shows larger Vtrip variation (Fig. 5(b)) and σRSNM than the (110,100,110) cell. The voltage margin between Vread,0 and Vtrip is larger in the (110,100,110) cell than the (100,100,110) one, which indicates the μRSNM is larger in the (110,100,110) SRAM cell. Therefore, the (110,100,110) SRAM cell shows larger μRSNM/σRSNM than the (100,100,110) one. (PU,PD,PG) = (110,110,110) SRAM cell shows higher σRSNM than the (100,100,110) cell because the (110) NFET with stronger quantum confinement shows larger threshold voltage variation due to fin LER than the (100) NFET. (110,110,110) SRAM cell with both (110) PD and PG devices shows larger Vread,0 variation and degrades the RSNM variability (Fig. 5(b), bottom).

Fig. 6(a) compares the normalized σWSNM and μWSNM/σWSNM. (PU,PD,PG) = (100,100,110) SRAM cell shows larger Vwrite,0 variation, Vtrip variation (Fig. 6(b)) and σWSNM due to larger variations of (100) PU and (110) PG devices. However, (100,100,110) SRAM cell still shows higher μWSNM/σWSNM due to its larger μWSNM.

*B. Long-Term Stability/Variability due to NBTI/PBTI*

Degradation in SRAM stability with time under worst-case stress pattern/condition (extreme asymmetry condition, only PR with NBTI and NL with PBTI) is considered (Fig. 7). Fig. 8 (a) and (b) shows the time-dependent threshold voltage increase ($|\Delta V_{th}|$) due to NBTI and PBTI for $SiO_2/HfO_2/TiN$ and $SiO_2$ FETs respectively and the insets demonstrate the good calibration results with published data [7, 8]. For $SiO_2/HfO_2/TiN$ FETs, PBTI and NBTI induced Vth shifts are comparable. For $SiO_2$ FETs, NBTI induced $|\Delta V_{th}|$ is larger than PBTI by ~1 order of magnitude for the poly-gate FinFETs studied. Fig. 9 shows that FinFET SRAM cells with $SiO_2$ dielectric suffer from NBTI and show 9.5% degradation in RSNM due to its decreased Vtrip. FinFET SRAM cells with high-k metal gate suffer from NBTI/PBTI and show 33.5% degradation in RSNM due to its increased Vread,0 and decreased Vtrip (Fig. 9 inset). The sensitivity of PBTI on RSNM is larger than NBTI. Fig. 10 shows the impact of NBTI/PBTI induced $|\Delta V_{th}|$ on the RSNM. FinFET SRAM cells with (110)-oriented PD(PU) devices suffer larger NBTI(PBTI) degradation due to higher number of interface traps, resulting in larger degradation in RSNM. In contrasted with the significant RSNM degradation due to NBTI/PBTI, Fig. 11 and 12 show that the WSNM only degrades slightly. NBTI weakens PR and makes VR easier to write than VL, therefore, WSNM is mainly determined by writing VL. The long-term WSNM variability degrades slightly as compared with the short-term WSNM variability. Fig. 13 shows the long-term RSNM variability considering LER and NBTI/PBTI induced $V_{th}$ variation. PBTI dominates the RSNM variation for high-k metal gate SRAM cells, thus, SRAM cells with (110) PD devices show larger σRSNM, Vread,0 variation (Fig. 14 bottom) and Vtrip variation (Fig. 15 bottom). However, for $SiO_2$ FETs, NBTI dominates its RSNM variation, thus, SRAM cells with (110) PU devices show decreased μRSNM (Fig.10 inset) and larger σRSNM (Fig. 13 inset). Therefore, SRAM cells ($SiO_2$ dielectric) with (110) PU devices show larger decrease in μRSNM/σRSNM than SRAM cells with (100) PU devices. Fig. 16 demonstrates that NBTI/PBTI induced temporal variability in SRAM will change the optimal choice of FinFET SRAM cells with different gate stacks in terms of μRSNM/σRSNM.

In summary, the time-dependent $V_{th}$ drift and variation due to NBTI/PBTI degrades the stability/variability of RSNM (significantly) and WSNM (slightly). Our study indicates that optimum FinFET SRAM design has to consider the combined effects of intrinsic process variability and the temporal variability introduced by NBTI/PBTI.

## Acknowledgement

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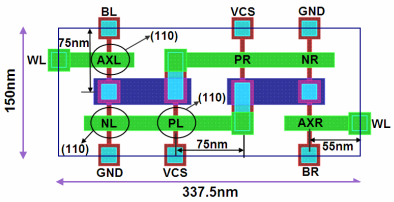



Fig. 1. (a) Pull-up (PL/PR), pull-down (NL/NR) and pass-gate transistors (AXL/AXR) all with (110) orientation.

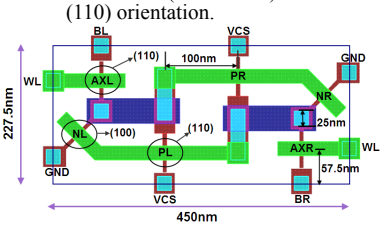



Fig. 1. (b) (110) pull-up, (100) pull-down and (110) pass-gate transistors.

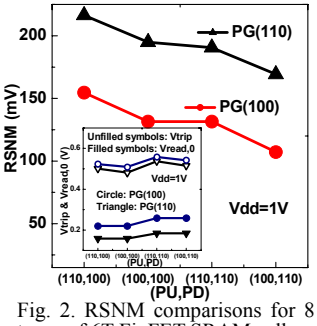



Fig. 2. RSNM comparisons for 8 types of 6T FinFET SRAM cells.

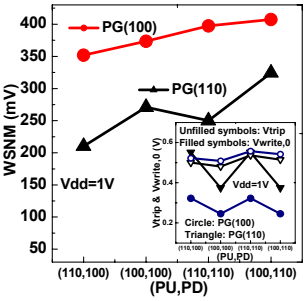
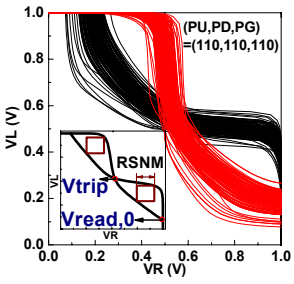



Fig. 3. WSNM comparisons for 8 types of 6T FinFET SRAM cells.



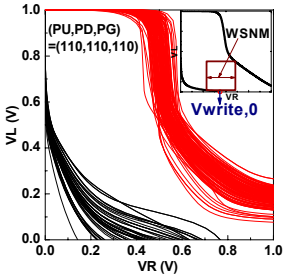




Fig. 4. (a) RSNM variation, and (b) WSNM variation due to fin LER. (correlation length=20nm, rms amplitude =1.5nm [9]).

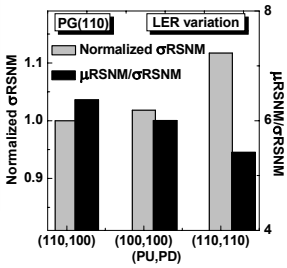



Fig. 5. (a) Normalized σRSNM and μRSNM/σRSNM comparison considering fin LER. (110,100,110) SRAM cell shows largest μRSNM/σRSNM.

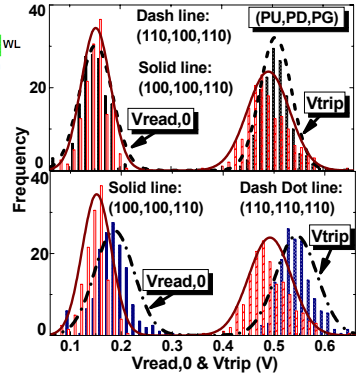



Fig. 5. (b) Vread,0 and Vtrip variation comparisons considering fin LER.

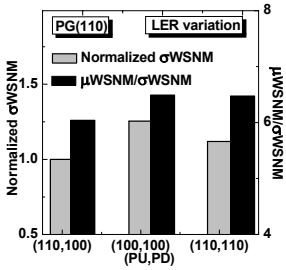



Fig. 6. (a) (100,100,110) SRAM cell shows largest μWSNM/σWSNM.

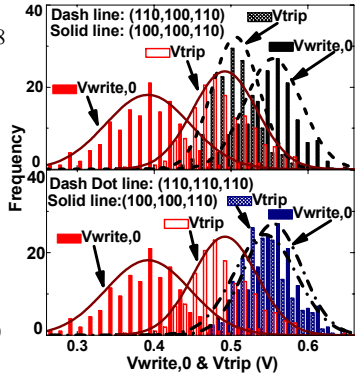



Fig. 6 (b) Vwritet,0 and Vtrip variation comparisons considering fin LER.

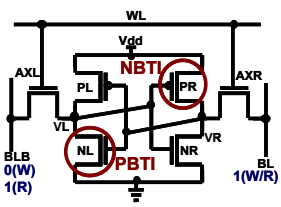



Fig. 7. Worst case stress scenario for Read (R) and Write (W) stability.

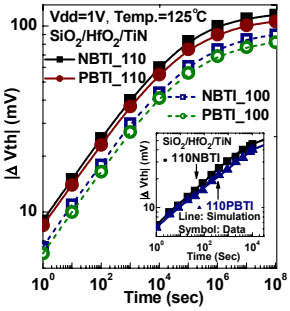



Fig.8(a).NBTI/PBTI induced $V_{th}$ shift for $SiO_2/HfO_2/TiN$ FET. Inset shows the model-data calibration.

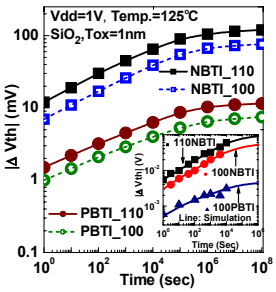



Fig.8(b)BTI induced $V_{th}$ shift for $SiO_2$ gate dielectric FET.

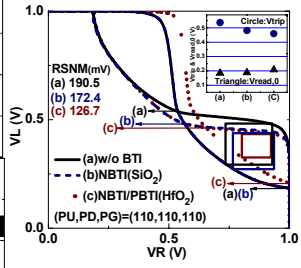



Fig. 9. RSNM comparison among curves (a) w/o BTI, (b) considering NBTI only and (c) considering NBTI/PBTI. Stress time is $1x10^8$ sec. @ 125℃.

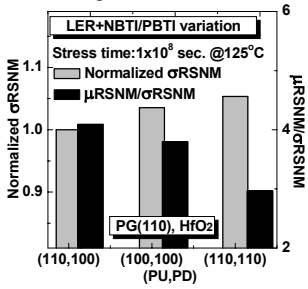



Fig. 13. (110,100,110) SRAM cell ($HfO_2$) shows largest μRSNM/σRSNM.

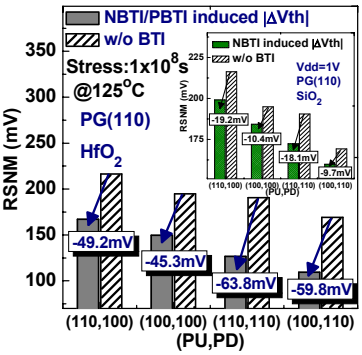



Fig. 10. (a) RSNM degradation due to NBTI/PBTI. Inset shows the RSNM degradation due to NBTI only.

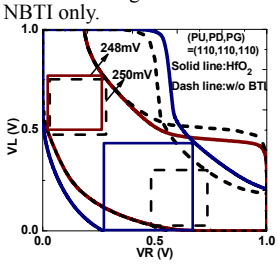



Fig. 11. WSNM comparison between SRAM cells w/o BTI and considering NBTI/PBTI. Stress time is $1x10^8$ sec. @ 125℃.

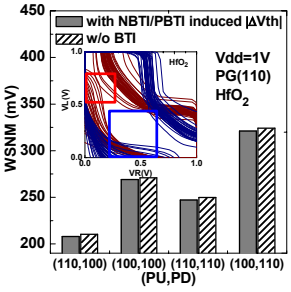



Fig. 12. Slight degradation in WSNM due to NBTI/PBTI under worst case stress condition. NBTI/PBTI stress time is $1x10^8$ sec. @ 125℃.

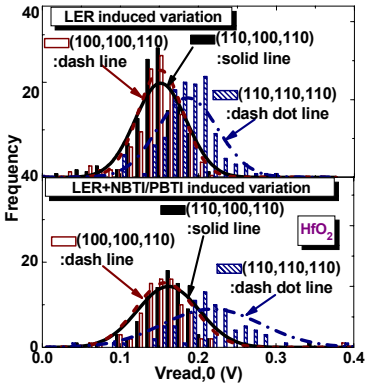



Fig. 14. (110) PD devices show larger time-dependent Vread,0 variability degradation and Vread,0 increasing. BTI stress time is $1x10^8$ sec. @ 125℃.

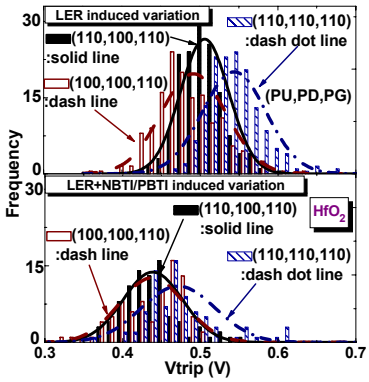



Fig. 15. (110) PD devices show larger time-dependent Vtrip variability degradation. BTI stress time is $1x10^8$ sec. @ 125℃.

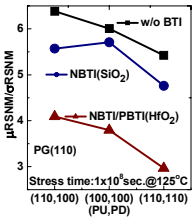



Fig. 16. μRSNM/σRSNM comparison considering short-term (fin LER) and long-term (fin LER + NBTI/PBTI) variations.