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FinFETs Junctions Optimization by Conventional Ion Implantation for (Sub-)22nm Technology Nodes Circuit Applications

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Abstract

In this work we explore several doping schemes for aggressively scaled FinFET devices (H_{Fin}~37nm, W_{Fin}≥10nm, L_g≥30nm), using conventional ion implantation, and suitable for both logic and dense circuit applications. We demonstrate that low-energy and: 1) low-tilt, double-sided extension(-less) I/I, or 2) high-tilt, single-sided extension I/I schemes can enable pitch scaling without resist shadowing effects, with no penalty in device performance and yielding higher 6T-SRAM SNM values. Key advantages of the extension-less approach are: reduced cost & cycle time with 2 less critical I/I photos, enabling better quality, defect-free growth of Si-epitaxial raised S/D (SEG), and up to 20× lower I_{OFF}. It, however, requires a tight spacer CD control, a less critical parameter for the single-sided I/I scheme, which also allows wider overlay margins.

Introduction

FinFET-based multi-gate (MuGFET) devices are considered one of the most promising device architectures for enabling further CMOS scaling beyond the 32nm technology node, thanks to their improved electrostatics and steeper sub-threshold slopes, with reduced V_T variability due to lower channel dopants concentration [1-8]. This makes them particularly attractive for helping prolong SRAM scaling, facing ever-increasingly challenges with maintaining acceptable noise margins and controlled instability. However, FinFET parasitics remain a concern, requiring reduction of the series resistance R_{SD} through improved Fin morphology and Fin doping [5,9]. For ion implanted junctions, this issue is greatly aggravated by tilt angle restrictions due to resist shadowing in tight pitch structures. Recently, to reduce non-uniformity of implanted dosage in the Fins in an SRAM cell, responsible for characteristic variability degradation, a single-sided I/I scheme was proposed, reporting stable SRAM operation,but lower drive current compared to the double-sided I/I case due to higher extension resistance [4].

In this paper, using conventional ion implantation, several doping strategies for highly scaled FinFET devices are evaluated for improved variability control at denser pitches, with no penalty in performance, leakage nor Short-Channel-Effects (SCE), and with demonstrated scalability for (sub-)22nm circuits (RO and SRAM).

Device fabrication

A schematic of the process flow used for device fabrication is shown in Fig.1, starting with SOI thinning down to ~40nm to allow a more robust gate patterning process at scaled pitches. A corner rounding step to remove etch-induced Si damage and smoothen the Fin sidewalls follows Fin patterning (W_{Fin}≥10nm). HfSiON/TiN gate stack, capped with a-Si and CET~2.2nm, is patterned using an oxide/α-C/SiOC hard-mask (HM). Extensions I/I were preceded by a thin oxide liner deposition, at 200°C, to reduce dose loss during strip. Extension-less devices were fabricated with a narrower 1st (HDD) spacer (CD≤12nm after SEG) and thinner, ~23nm-thick SEG (Fig.2). With addition of a 2nd spacer, total spacer width prior to silicidation is similar for all devices.

Device characteristics and Circuits results

Fig.3 illustrates the two implant options considered for dense Fin pitches to avoid shadowing effects: a) low-tilt, double-sided I/I and b) high-tilt, single-sided I/I. Extension-less devices using the 1st approach (low-tilt, 2Q HDD I/I) were also investigated, starting with simulations *vs.* reference devices (Fig.4) for assessing the impact of several process parameters changes, such as spacer width variations, in junctions profile and device characteristics.

R_{SD} extracted for NMOS and PMOS devices, at relaxed pitch, for the different I/I options are shown in Fig.5. With optimized I/I conditions, no resistance penalty is obtained for single- *vs.* double-sided extension I/I. As for the extension-less devices, the better quality, defect-free SEG obtained when starting from undoped Fins [8,9] means that low R_{SD} values can be obtained with thinner SEG, with margin for further improvement by increasing its growth time, and potentially resulting in less R_{out} variability [5]. Regarding device performance, Fig.6 shows that optimized extension-less devices exhibit lower I_{OFF} values, consistent with the expected reduced gate overlap, also controlled to avoid high increase in R_{SD}. Excellent SCE behavior is obtained (Fig.7), corresponding to comparable (PMOS) or even slightly higher performance in NMOS devices: ~8% drive current increase at fixed I_{OFF}=100nA/μm (Fig.8). An overview of the ITP characteristics of PMOS devices fabricated with the different doping schemes is shown in Fig.9. Comparable performance can be obtained with (B 0.8keV) single-sided, 25° tilt extension I/I *vs.* double-sided, 45° tilt extension I/I, compensating the dopant loss at lower I/I angles with a small dose adjustment. These asymmetrically doped PMOS devices also outperform low-tilt I/I devices in about ~7-10% higher I_{ON} at I_{OFF}=100nA/μm. The I_D-V_G curves in Fig.10 (NMOS devices for different doping strategies) highlight again the lower off-state current of extension-less devices *vs.* the other implant strategies, corresponding to a lower DIBL~36mV/V and SS~70mV/dec. Fig.11 shows that for both NMOS and PMOS devices, tight V_T distributions ($\sigma(V_{Tlin})$≤20mV) can be obtained for the different I/I schemes (data at relaxed pitch, without shadowing effects impact).

Implementation into Ring Oscillators (Fig.12; data shown for ROs with 12 and 16 Fins for NMOS and PMOS devices, respectively) shows that comparable performance can be obtained for single- *vs.* double-sided, high-tilt extension I/I devices with optimization of the implant conditions. On the other hand, lower static power dissipation is obtained for low-tilt I/I devices.

In agreement with the tight distributions in Fig.11, comparable V_T-mismatch results ($\sigma(\Delta V_T)$≤30mV) are shown in Fig.13 for aggressively scaled Pull-Down (PD), Pass-Gate (PG) and Pull-Up (PU) transistors of relaxed SRAM cell sizes, for the different doping schemes. This is, of course, due to the fact that, in this case, shadowing effects are of no concern. However, the correspondent cells SNM values shown in Fig.14 are clearly higher for the low-tilt I/I and high-tilt, single-sided extension I/I schemes, the most suitable doping approaches for scaled, denser cells. Improved operating margin can also be achieved by increasing the cell β ratio from 1 to 1.7, through an increase in the gate length for the PG transistor, as shown in Fig.14 (right plot). Overall, successful SRAM operation requires good SCE, low leakage, and a robust contact module. The extension-less approach, exhibiting lower off-state current, while keeping low R_{SD}, can then be particularly attractive for scaled cells. Butterfly curves of a 22nm node 6T-SRAM cell (0.099μm^2 cell size [8]) successfully built up with this approach are shown in Fig.15, with SNM>0.1V_{DD} down to 0.6V.

Conclusions

This work demonstrated a junctions formation methodology for aggressively scaled FinFET devices, using conventional ion implantation, and compatible with dense pitches applications, without penalty in R_{SD} nor device performance, and yielding higher SRAM SNM values: 1) low-energy & low-tilt, double-sided extension(-less) I/I approach, with key advantages in terms of cost & cycle time, better quality, defect-free SEG, and lower I_{OFF} when skipping extensions; or 2) low-energy & high-tilt, single-sided extension I/I scheme, less sensitive to resist profile and allowing wider overlay margins (higher scalability), with the design constrain of needing to account for isolated/dense differences.

References

[1] J. Kavalieros *et al.*, VLSI *Tech. Dig.* 2006, 62; [2] S. Inaba *et al.*, IEDM *Tech. Dig.* 2007, 487; [3] N. Collaert *et al.*, ICICDT *Tech. Dig.* 2008, 59; [4] H. Kawasaki *et al.*, IEDM *Tech. Dig.* 2008, 237; [5] T. Mérelle *et al.*, IEDM *Tech. Dig.* 2008, 241; [6] A. Veloso *et al.*, IEDM *Tech. Dig.* 2008, 861; [7] C.-Y. Chang *et al.*, IEDM *Tech. Dig.* 2009, 293; [8] A. Veloso *et al.*, IEDM *Tech. Dig.* 2009, 301; [9] R. Duffy *et al.*, *Appl. Phys. Lett.* 90, 241912, 2007.

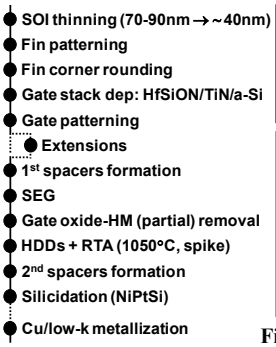

Fig.1 – Schematic of process flow used for device fabrication on 300mm (100) SOI wafers.

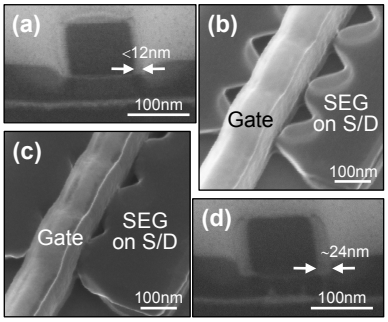

Fig.2 – SEM and FIB images of MuGFET devices after raised S/D by Si-epitaxial growth (SEG) and gate oxide-HM partial removal: (a,b) for extension-less devices (undoped Fins); (c,d) for reference devices with wider 1st spacers and thicker SEG.

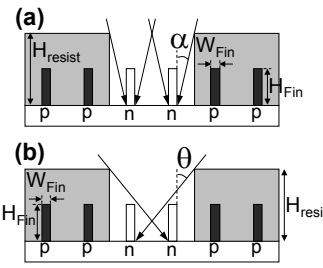

Fig.3 – Ion implantation strategies evaluated for dense Fin pitches (e.g., for dense SRAM fabrication): (a) low-tilt, double-sided I/I; and (b) high-tilt, single-sided I/I. Implant angles α and θ are limited by the resist height, Fin height and pitch, and overlay.

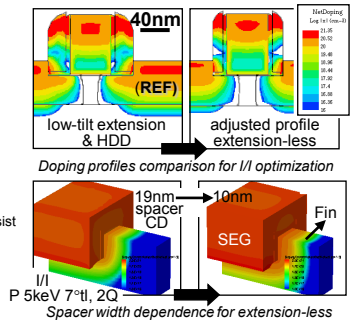

Fig.4 – On top, contours of net active doping for extension-less *vs.* reference devices. At the bottom, evaluating the impact of spacer width on extension-less devices, for P 5keV 7° tilt, 2Q I/I.

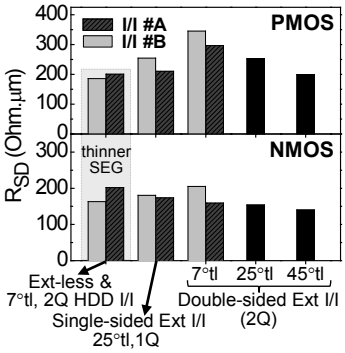

Fig.5 – R_{SD} for NMOS and PMOS MuGFETs [5-Fins devices, with W_{Fin}~15nm, H_{Fin}~37nm, and $W_{effective}$= 5×(2×H_{Fin}+W_{Fin})]. R_{SD} was extracted by extrapolating to L_g=0 the total resistance R measured at $|V_{GS}-V_{Tlin}|$ =2V and $|V_{DS}|$=20mV.

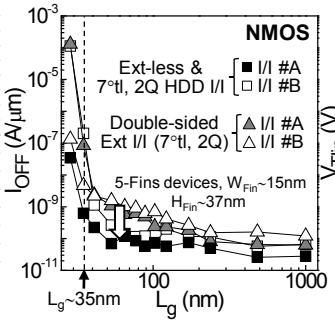

Fig.6 – Upon I/I optimization, extension-less devices exhibit lower off-state current down to narrower gates (L_g~35nm). They have narrower HDD spacers but, after addition of a 2nd spacer, the total spacer width prior to silicidation is similar for devices of both I/I schemes.

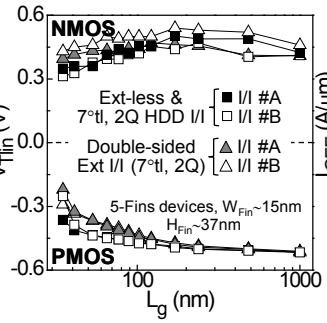

Fig.7 – Comparable (or even sligthly better, for PMOS) V_{Tlin}-L_g roll-off behavior is obtained for extension-less devices *vs.* reference devices (fabricated with low-energy & low-tilt, double-sided extension I/I).

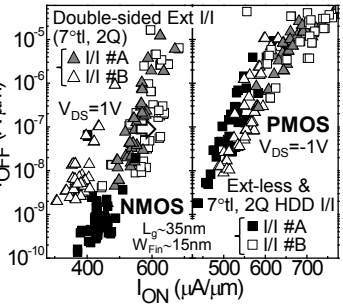

Fig.8 – Extension-less NMOS devices show improved drive current at fixed I_{OFF} *vs.* reference devices (fabricated with low-tilt, double-sided As extension I/I & (As+P) HDD I/I). For PMOS devices, comparable performance can be obtained with optimized B implant conditions.

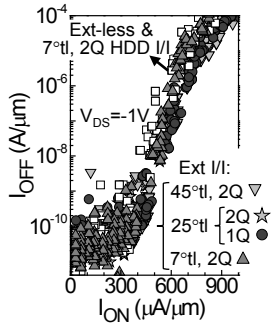

Fig.9 – ITP characteristics of PMOS devices fabricated with different doping strategies (5-Fins devices; W_{Fin}~15nm, H_{Fin}~37nm). Comparable performance is obtained for optimized single-sided *vs.* double-sided, high-tilt extension I/I.

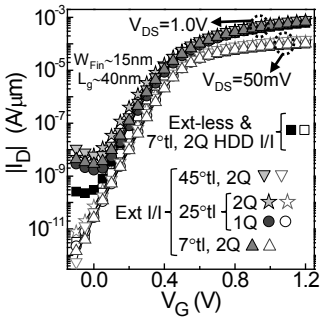

Fig.10 – I_D-V_G curves of NMOS 5-Fins devices for different I/I strategies (W_{Fin}~15nm, H_{Fin}~37nm). 6× to 20× lower I_{OFF} is obtained for extension-less devices.

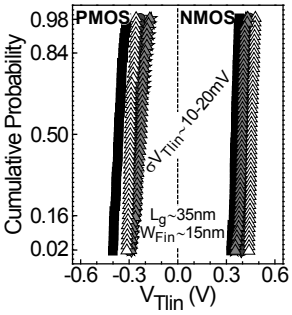

Fig.11 – Tight V_{Tlin} distributions can be obtained with the different low-energy I/I strategies: low-tilt, double-sided extension-less I/I (■); low-tilt (▲△) *vs.* high-tilt (★▽), double-sided extension I/I; and high-tilt, single-sided extension I/I (●).

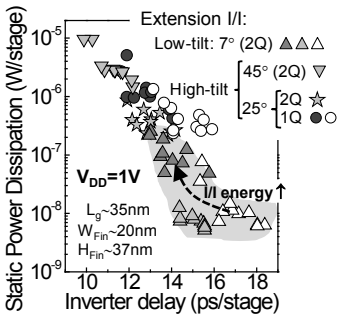

Fig.12 – Ring Oscillators fabricated with optimized single-sided *vs.* double-sided, high-tilt extension implants have comparable performance (data shown here for ROs with 12 Fins for NMOS, 16 for PMOS).

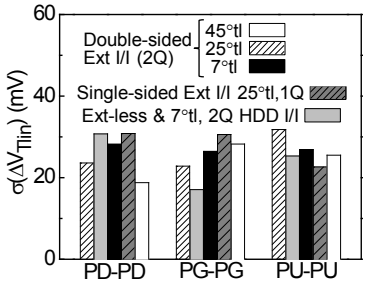

Fig.13 – $\sigma(\Delta V_{Tlin})$ for Pull-Down (PD), Pass-Gate (PG) and Pull-Up (PU) transistors of 6T-SRAM cells of relaxed size, for the different implantation options under evaluation. (Devices with W_{Fin}~10nm and L_g~30-35nm.)

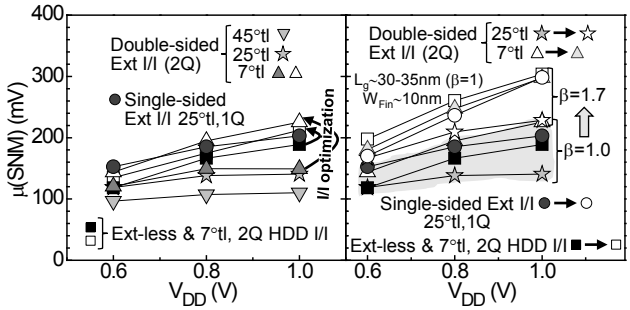

Fig.14 – SNM values of 6T-SRAM cells of relaxed size, using different I/I schemes to dope the cell transistors. Higher values are obtained with: 1) double-sided, low-tilt I/I (w/ and w/o extensions), and 2) single-sided, high-tilt extension I/I, with both approaches being also the most suitable for denser pitches to avoid resist shadowing.

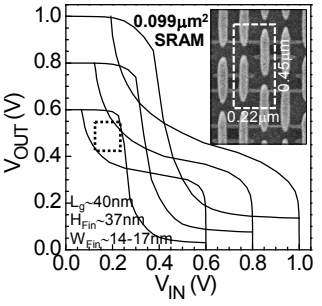

Fig.15 – Butterfly curves of a 22nm node 6T-SRAM cell, using extension-less devices for the cell transistors [W_{Fin}(PU, PD)~17nm, W_{Fin}(PG)~14nm, and L_g~40nm].