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Using Power Transform to Study DC and AC CHC Effects on nMOSFETs in 65 nm Technology

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1. Introduction

As the shrinking of the device size, channel hot-carrier (CHC) is the most critical reliability issue on MOSFETs in CMOS technology [1-3]. It is well-known that DC HC reliability test is usually executed with constant voltage stress (CVS) to investigate MOSFET degradation and to evaluate device lifetime (τ) in wafer foundry. It is because the engineers hope to shorten the testing time for evaluating the device yield.

However, MOSFETs are generally operated at AC mode in CMOS circuit. So, many researchers studied how to switch the τ from DC mode to AC mode (i.e., τ_{DC} to τ_{AC}) and found the DC to AC lifetime factor for quick-predicting the τ_{AC} of in-circuit devices [4-6]. From these researches, some problems still can be found and showed as follows:

(a) The τ_{AC}/τ_{DC} lifetime factor which the researches reported is only suitable for some circuit applications due to different AC operation signals. The adaptability is not good enough.

(b) The investigations of lifetime models are based on current stress or voltage stress. They seem to have questions in theory.

(c) Early studies may be past. It is hard to suit the high temperature CHC issue on nMOSFETs of 65 nm node and beyond.

To avoid the foregoing problems, for the first time, this work is to propose a new idea, power transform, and to respectively investigate nMOSFET degradation after DC and AC CHC stress. The power transform model is established as a function of voltage, current, and temperature. Furthermore, the DC and AC CHC results show that power transform model can fit the experimental data for different stress conditions.

2. Experiment and result discussions

All the tested nMOSFETs were fabricated using 65 nm process of UMC. The gate width/length (W/L) is equal to 1/0.05 (μm). The gate dielectric is SiON and oxide thickness (T_{ox}) is around 19.5 Å. During DC and AC CHC stress, nMOSFET properties including threshold voltage (V_t) and saturation current ($I_{d,sat}$) are extracted by using Keithley 4200 SCS and Agilent 81101A pulse generator and analyzed with different stress conditions. For AC case, the trapezoid waves including different period T (T_{pd}) = 4, 8, and 16 ms are as the AC stress signal and the duty cycle is 50 %.

For DC CHC case, Figure 1 shows that V_t shifts versus stress time on nMOSFETs with different stress voltages and temperatures. The results show that the degradation induced by CHC is clearly serious with increasing stress time. The worst case occurred at high stress voltage and temperature. Figure 2 shows the curves of $I_{d,sat}$ degradation-temperature with the same stress conditions. CHC stress at high temperature has the worst degradation.

For AC CHC case, Figure 3 shows V_t shifts versus stress time on nMOSFETs with different stress voltages and temperatures. Compared with the results of Fig. 1, DC CHC stress is more serious than AC CHC stress. Also, the high temperature case is worse than the low temperature case. Figure 4 shows that the degradation of $I_{d,sat}$ versus temperature with the same stress conditions. Similarly, compared with the results of Fig. 2, the degradation of $I_{d,sat}$ due to AC CHC stress is slighter than that of DC CHC stress.

In this work, the power transform opinion is used to form a new model and to describe DC and AC CHC-induced nMOSFET degradations. Considering the contribution of V_d, V_g-V_t, I_d, and I_g, the total transformed power (P_{total}) is calculated, respectively for DC and AC CHC stress. Then, P_{total} can be expressed as

$$P_{total} = A_1 V_d I_d + A_2 (V_g - V_t) I_g \quad (1)$$

Moreover, according to our previous studies [2, 3], the degradation model can be showed as:

$$\Delta V_t = A t^n \exp[-(\frac{1}{P_{total}} + \frac{\gamma}{kT})] \quad (2)$$

where P_{total} is the total transformed power, A_1 and A_2 are the fitting constants, n is the time power law, γ is the thermal activation energy, k is the Boltzmann's constant. All the related parameters of nMOSFETs for DC and AC CHC stress are showed in Table 1.

Figure 5 shows the curves of V_t shifts-$V_d I_d$ in CHC at 85 °C. Separately, the fitting constants, A_1, are about 107.13 W^{-1} for DC case and 150.29 W^{-1} for AC case. Similarly, Figure 6 shows the curves of V_t shifts-$(V_g$-$V_t)I_g$ in CHC at 85 °C. The A_2 for DC and AC cases are around 6.17×10^8 W^{-1} and 7.66×10^8 W^{-1}, respectively. Figure 7 shows the curves of V_t shifts-temperature in DC and AC CHC with different stress conditions. The thermal activation energy (γ) between DC and AC CHC stress is so close (~ 0.032 eV).

Figure 8 shows the comparisons of the experimental results and power transform model fitting in DC CHC at different stress voltages and 125 °C. The DC data shows the good fitting. On the other hand, Figure 9 shows the experimental results and model fitting data in AC CHC with different T_{pd} of the trapezoid wave. Furthermore, all the AC CHC data is well fitted with power transform method. Figures 10 and 11 respectively show the predicted lifetimes after DC and AC CHC stress at different stress conditions. Compared the lifetime predictions at operation region, the results show the AC CHC lifetime is better than DC CHC lifetime.

3. Conclusions

For the first time, this article is to use power transform to describe nMOSFET degradation due to DC and AC CHC stress. The power transform model is a function of voltage (V_d, V_g-V_t), current (I_d, I_g), and temperature (T). In DC case, the most severe nMOSFET degradation is at the higher stress voltage and temperature. In AC case, the AC stress signal with lower T_{pd} causes the most severe nMOSFET degradation. All the results show that the power transform model can well fit the experimental data of DC and AC CHC stress. The significance of this work is to clearly give wafer foundries and design houses the total transformed power (P_{total}) which causes device failure to understand the τ of in-circuit devices. It is not only to reduce the testing time but also improve the work efficiency.

References

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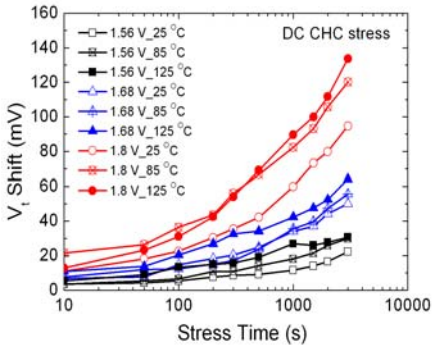

Fig. 1. The curves of V_t-stress time (t) on nMOSFETs in DC CHC at different stress voltages and temperatures.

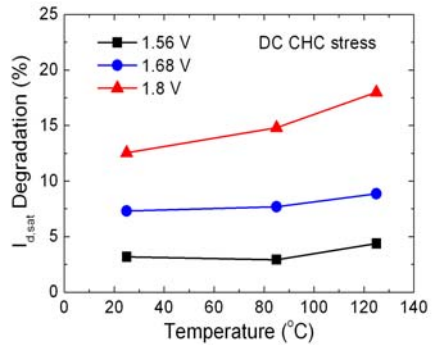

Fig. 2. The $I_{d,sat}$ degradation versus temperatures on nMOSFETs in DC CHC with different stress conditions.

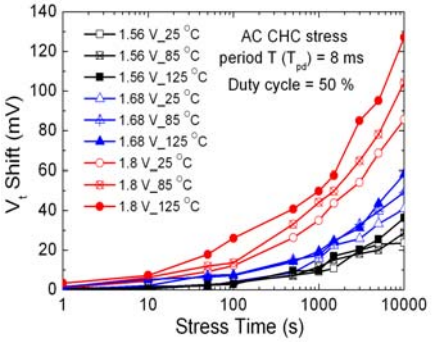

Fig. 3. The curves of V_t-t on nMOSFETs in AC CHC at different stress voltages and temperatures.

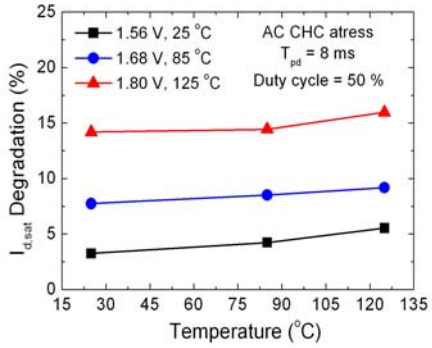

Fig. 4. The $I_{d,sat}$ degradation versus temperatures on nMOSFETs in AC CHC with different stress conditions.

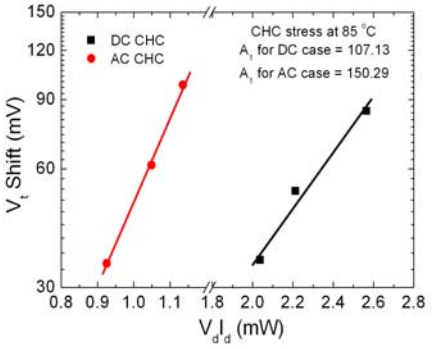

Fig. 5. The curves of V_t shift-V_dI_d in DC and AC CHC with different stress voltages at 85 °C. The A_1 can be extracted.

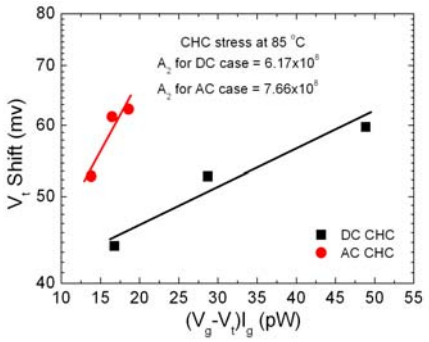

Fig. 6. The curves of V_t shift-$(V_g$-$V_t)I_g$ in DC and AC CHC with different stress voltages at 85 °C. The A_2 can be extracted.

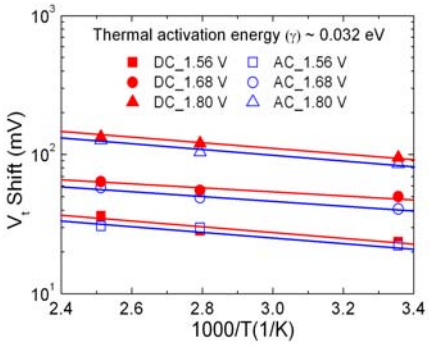

Fig. 7. The V_t shifts-temperature characteristics in DC and AC CHC with different stress conditions.

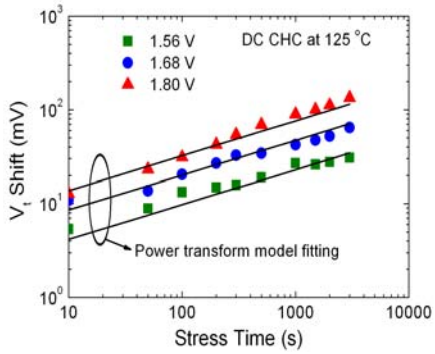

Fig. 8. The comparisons of the results and power transform model fitting in DC CHC at different stress voltages and 125 °C.

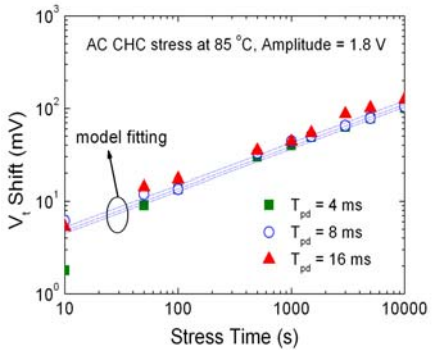

Fig. 9. The experimental and model fitting results in AC CHC with different T_{pd} of the trapezoid wave.

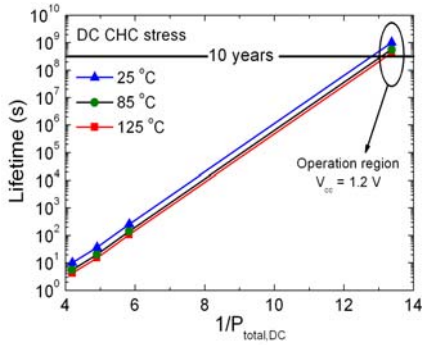

Fig. 10. The predicted lifetimes at operation region after DC CHC stress at different temperatures.

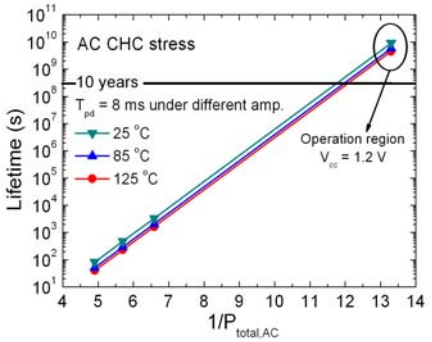

Fig. 11. The predicted lifetimes at operation region after AC CHC stress at different stress conditions.

Table 1. The related parameters on nMOSFETs in DC and AC CHC by using power transform method.

Stress mode	CHC	
Stress type	DC stress	AC stress
A_1 (W^{-1})	107.13	150.29
A_2 (W^{-1})	6.17×10^8	7.66×10^8
γ (eV)	0.032	0.032