Investigation of Recovery Effects on Degraded pMOSFETs of 65 nm Technology with Different Annealing Temperatures

Shuang-Yuan Chen1,*, Chia-Hao Tu1, Ying-Fu Chen1, Heng-Sheng Huang1, Zi-Wei Jhou2, Sam Chou2, and Joe Ko2

1Institute of Mechatronic Engineering, National Taipei University of Technology
No. 1, Sec. 3, Chung-Hsiao E. Rd., Taipei 106, Taiwan
Phone: +886-2-2771-2171 ext: 2011 Fax: +886-2-2771-7318 E-mail: sychen@ntut.edu.tw
2Integration Technology Division, United Microelectronics Corporation

1. Introduction

It is well-known that the MOSFET degradation after CHC and NBTI stress is due to the increment of interface states (ΔN_{it}) and oxide trapped charges (ΔN_{ox}). Early researches thought that CHC-induced MOSFET degradation refers to the breaking of Si-H bonds to increase ΔN_{oi} and ΔN_{ox} [1-2]. Some researches indicated that hole trapping is dominant for NBTI-induced MOSFET degradation. Their recovery effect also catches much attention [3-4]. The mechanisms of degradation and recovery are involved with trapping and detrapping of Not and Nit [3-4]. The cause is supposed that the Si-H bonding force is so weak to easily make Si dangling bond and the H related species may diffuse into gate dielectric to create more Not. However, for detrapping or recovery, there is no acceptable model that can be applied. Recently, a research revealed that bake at 325 °C after NBTI stress will produce full recovery, but the major mechanism is still unclear [7].

The degradation or recovery effects of MOSFET properties seem not entirely assure to come from the variation of the broken Si-H bonds. In 2009, our study indicated that ΔN_{oi} can be clearly recovered with high temperature annealing [8]. So, it is necessary to further understand the recovery effect in 65 nm node and beyond.

In this work, both CHC and NBTI stresses are checked to investigate the recovery mechanism with different temperature annealing. The variations of threshold voltage (Vt), saturation current (Idsat), and transconductance (gm) of pMOSFETs were measured. By using subthreshold swing method (SS method), the variations of interface state density (ΔD_{ox}) are also estimated.

2. Experiment and result discussions

All the tested pMOSFETs were fabricated using 65 nm process of UMC. The gate oxide is SiON with oxide thickness (Tox) of 19.5 Å. The gate width/length (W/L) is equal to 10/0.06 (μm). The CHC and NBTI stress conditions are performed at stress voltage (V_{stress}) = -1.8 V and 125 °C. Annealing treatment (AT) includes 100 % Not (AT1) and 85 % Not + 5 % Nit (AT2) and annealing conditions were performed at 250, 300, 350, and 400 °C for 30 min.

Figure 1 shows CHC and NBTI stress-induced ΔV_{t} degradation on pMOSFETs at -1.8 V and 125 °C. Clearly, CHC stress is worse than NBTI stress. Figure 2 shows the comparison of gm degradation in CHC and NBTI with the same stress condition. The results show that gm degradation induced by CHC is worse than that of NBTI. It means that the large quantity ΔN_{oi} should occur in CHC case. Respectively, Figs. 3 and 4 show the comparisons between ΔV_{t} (i.e., Vg shift) and ΔD_{ox} on pMOSFETs during CHC and NBTI stress under stress condition of -1.8 V and 125 °C. The ΔD_{ox} extracted by using SS method. From Figs. 3 and 4, the degradation trends of ΔV_{t} and ΔD_{ox} are so similar for CHC and NBTI stress modes. So, it is safely thought that ΔN_{oi} dominates pMOSFET degradation after CHC and NBTI stress.

Figure 5 shows the characteristics of ΔV_{t} and Ids Vict on fresh (unstressed) pMOSFETs before and after anneal, which shows the AT did not change the properties of unstressed pMOSFETs.

By measuring the curves of Idsat-Vg, Figs. 6 and 7 respectively show the comparisons of recovery ratio of Not and Nit incorporation (i.e., AT1 and AT2) with different annealing temperatures in CHC and NBTI cases. Recovery ratio is calculated from Idsat of (Annal-stress)/(Fresh-stress). Compared between Figs. 6 and 7, it is found that AT2-induced pMOSFET recovery is likely better in CHC than AT1, but this situation is not showed in NBTI.

On the other hand, Figs. 8 and 9 show the curves of gm-Vg after CHC and NBTI stress under different measurement points including Fresh, Stress, and Anneal. Recovery ratio is about 116.20 % and 83.44 % in AT2 of 400 °C, respectively for CHC and NBTI cases. It is known that the gm characteristic is correlated with the ΔD_{ox} at the SiON/Si-bulk interface. The ΔD_{ox} seems to be easily recovered under high temperature annealing. Then, by using SS method, Figs. 10 and 11 reveal that ΔV_{t} recovery is apparently dependent on ΔD_{ox} recovery after anneal. This cause may be due to the H related species staying near the SiON/Si-bulk interface. The results are contrary to the viewpoint of standard R-D model [5]. The standard R-D model may be carefully reexamined.

Figure 12 shows the hydrogen (H) concentration profiles of this work and standard R-D model. In R-D model, the assumptions of regarding the initial condition of the H concentration is zero and certain boundary is zero just did not reflect the real situation [9]. In this work, the initial condition is modified and the H concentration increases from SiON/Si-bulk to SiON/poly-Si interface. Also, the boundary condition is modified at the situation of finite oxide thickness. Moreover, as for the slope (n value) variations of degradation (e.g. ΔV_{t}), they may be only due to different bonding energy resulted from strained bonding [10].

3. Conclusions

In this article, CHC and NBTI-induced pMOSFET degradation is almost recovered after high temperature anneal. The results prove that ΔN_{oi} can be recovered and dominates the improvement of pMOSFET properties. Thus, the recovery of large quantity ΔN_{oi} after anneal is conjectured to be due to most of the H related species staying near the SiON/Si-bulk interface. So, this work is considered that only reaction-limited regime takes place during the degradation and recovery phases, minor or no diffusion-limited regime has occurred simply maybe because the H related species are abundant around the interface. The assumptions of regarding the initial condition of the concentration of the H related species is zero and certain boundary is zero just did not reflect the real situation.

References

Fig. 1. The curves of $I_{ds}$ degradation-stress time on pMOSFETs in CHC and NBTI at stress voltage ($V_{stress}$) = -1.8 V and 125°C.

Fig. 2. The curves of $g_m$ degradation-stress time on pMOSFETs in CHC and NBTI at -1.8 V and 125°C.

Fig. 3. The comparison between $\Delta V_t$ and $\Delta D_{it}$ on pMOSFETs in CHC with stress condition of -1.8 V and 125°C.

Fig. 4. The comparison between $\Delta V_t$ and $\Delta D_{it}$ on pMOSFETs in NBTI with the same stress condition.

Fig. 5. The characteristics of $I_{ds}$-$V_g$ on fresh (unstressed) pMOSFETs before and after anneal.

Fig. 6. The comparisons of $I_{ds}$ recovery ratio with different annealing gases and temperatures in CHC case.

Fig. 7. The comparisons of $I_{ds}$ recovery ratio with different annealing gases and temperatures in NBRT case.

Fig. 8. The $g_m$-$V_g$ curves at different measurement points including Fresh, CHC stress and annealing conditions of H$_2$ and 400°C.

Fig. 9. The $g_m$-$V_g$ curves at different measurement points including Fresh, NBTI stress and annealing conditions of H$_2$ and 400°C.

Fig. 10. The comparison between $\Delta V_t$ and $\Delta D_{it}$ on pMOSFETs with CHC stress and annealing treatment of H$_2$ and 400°C.

Fig. 11. The comparison between $\Delta V_t$ and $\Delta D_{it}$ on pMOSFETs with NBTI stress and annealing treatment of H$_2$ and 400°C.

Fig. 12. The hydrogen (H) concentration profiles of this work and standard R-D model.