

## Gate Leakage Current Reduction in Two-Step Processed High-k Dielectrics for Low Power Applications

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### Abstract

Reduction of the gate leakage current in nMOS high-k devices is demonstrated by an engineered two-step deposited Hf-based high-k dielectric film. The electrical characteristics and reliability of the devices fabricated using the proposed two-step and conventional one-step high-k gate stacks are shown to be comparable. The lower leakage current is attributed to the misalignment of the grain boundaries in the multi-layer high-k dielectrics.

### Introduction

Hf-based high-k gate dielectrics have demonstrated they can meet the performance requirements for advanced technology nodes. However, reduction of the leakage current remains an important issue, specifically for low power applications. In this work, we demonstrate that engineered high-k dielectric stacks deposited in a two-step process exhibit an appreciable reduction in gate leakage current. The electrical characteristics and reliability of these two-step high-k devices are investigated, and the mechanism that contributes to the reduction in current is discussed.

### Experiment

N-channel MOSFETs with high-k gate dielectric films deposited using either a conventional one-step or two-step approach were fabricated for this study. For the one-step high-k stack, HfSiO<sub>x</sub> (10% SiO<sub>2</sub>) was grown by atomic layer deposition (ALD) followed by nitridation. For the two-step dielectric stack, the first ALD HfSiO<sub>x</sub> layer was followed by nitridation; afterward, the deposition/nitridation sequence was repeated for a second HfSiO<sub>x</sub> layer. The total physical thicknesses of the one and two-step high-k films, as well as the total nitride dosages, were the same. The TiN film was used as the transistor gate electrode; a spike anneal was applied to activate the source/drain dopant.

### Results and Discussion

Fig. 1 compares the capacitance-voltage (CV) characteristics of the one- and two-step high-k devices. The equivalent oxide thickness (EOT) of the two-step stack is only slightly less than that of the one-step stack with the same total physical high-k thickness, which suggests that the intentional interruption of the ALD has only a minimal effect on EOT. The electron energy-loss spectroscopy (EELS) data from the one-step and two-step high-k stacks, Fig. 2, indicate their similar chemical composition profiles. Fig. 3 shows the one-step and two-step high-k devices have comparable interface trap ( $N_{it}$ ) and bulk trap ( $N_{ot}$ ) densities. The time-zero breakdown (TZBD) voltages in accumulation for both types of devices are also similar, as shown in Fig. 4. The gate leakage current in the two-step high-k devices, however, is at least an order of magnitude lower than that of the one-step devices, Fig. 5, and is more than three orders of magnitude lower than that of the poly-SiO<sub>2</sub> stack, Fig. 6.

The above data show that the reduction in leakage current observed in the two-step high-k stack cannot be accounted for by the higher quality of its interface with the Si substrate [1] or lower density of the bulk high-k traps contributing to the trap-assisted tunneling (TAT) [2,3]. Since the grain boundaries (GBs) in the high-k layer were shown to form a conductive path [4], we suggest that the reduction in leakage current in the two-step high-k stack is caused by the misalignment of the GBs in two high-k layers; due to interrupted deposition/crystallization, the grains in each of the layers are expected to be formed independently, resulting in a disconnection of the single-GB conductive paths, some of which may propagate continuously through the single layer (one-step deposition) high-k film, as schematically shown in Fig. 7. To verify this model, conduction through the continuous and disconnected GB-related paths was simulated using the electron transport model, which considers a multi-phonon TAT mechanism [5]; the parameters of the traps, presumably oxygen vacancies precipitated at the GBs, used in the simulations were calculated within the DFT approach [6]. Fig. 8 compares the simulated gate leakage current results (using a single set of the trap parameters) and measurements for two sets of the high-k stacks with individual layers of different thicknesses. The excellent match between the simulation and measurement results supports the proposed GB misalignment model. Additional confirmation of the model was obtained by scanning tunneling microscopy measurements, which provided both topography and leakage current imaging of the dielectric stacks (see [7]).

The reduced leakage current in the two-step high-k stack is less prominent in inversion, especially at higher biases, Fig. 9, which can be understood using the energy band diagram, Fig. 10. In accumulation, the transport of the injected electrons can be facilitated by GBs in both layers, while under substrate injection at a higher  $V_g$ , the injected electrons mostly bypass one of the layers, resulting in greater leakage.

### Conclusion

A reduction of gate leakage current in the engineered high-k stacks deposited in two-steps is demonstrated. Lower gate currents are attributed to misalignment of the GBs in the two high-k layers. Electrical and reliability, Fig. 11, characteristics of the two-step high-k devices, which are comparable to those of conventional one-step devices, indicate that the two-step high-k stack is a promising candidate for low power applications.

**Reference.** [1] I.C. Chen et al., EDL, p.216 (1989). [2] K. Torii et al., IEDM, p.129 (2004). [3] J. Chen et al., IRPS, p.584 (2008). [4] K. S. Yew et al., SSDM (2009). [5] L. Larcher, IEEE TED 50,1246 (2003). [6] K. P. McKenna et al., APL 95, 222111 (2009), [8] K. S. Yew et al., SSDM (2010).

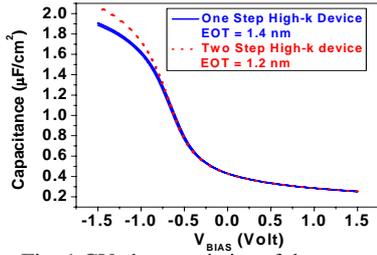


Fig. 1 CV characteristics of the one-step and two-step high-k devices

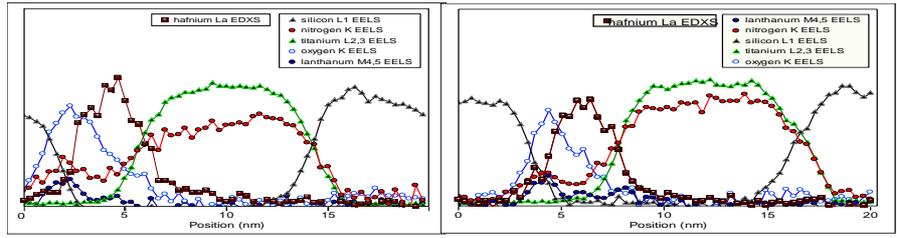


Fig. 2 The EELS profiles of the one-step (left) and two-step (right) high-k devices.

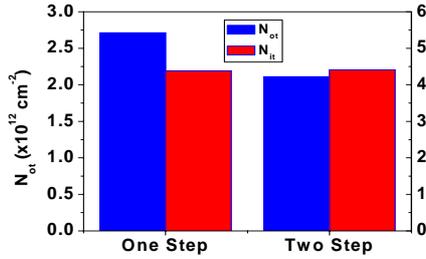


Fig. 3 Comparison of  $N_{it}$  and  $N_{ot}$  measured by the charge pumping at 1MHz and single pulse methods, respectively, for the one-step and two-step high-k gate stacks

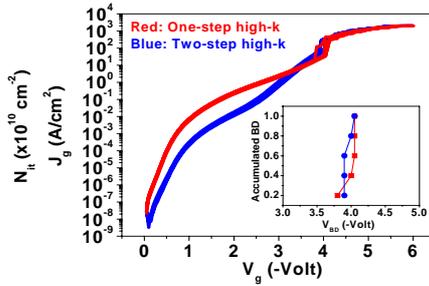


Fig. 4 TZBD characteristics and the  $V_{BD}$  distributions (inset) of the one-step and two-step high-k stacks.

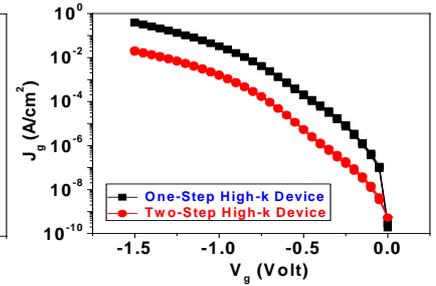


Fig. 5 The accumulation  $I_g$ - $V_g$  characteristics of the one-step and two-step high-k gate stacks.

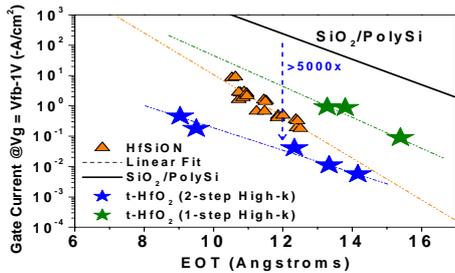


Fig. 6 The grand chart of the gate leakage current versus EOT for one-step and two-step high-k devices compared to poly/ $SiO_2$  devices

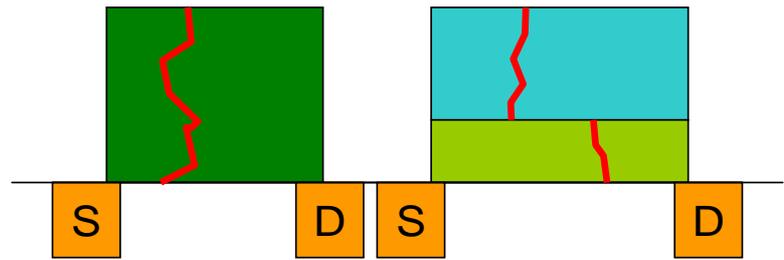


Fig. 7 Schematic illustration of the grain boundary alignment in one-step (left) and two step (right) high-k gate stacks.

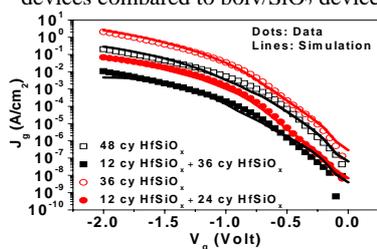


Fig. 8 The leakage current measurement data and simulation results for the one-step and two-step high-k gate stacks of different high-k thicknesses.

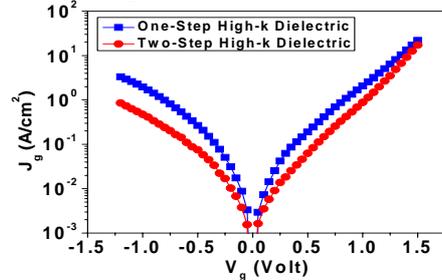


Fig. 9 The  $I_g$ - $V_g$  characteristics in inversion and accumulation for the one-step and two-step high-k stacks.

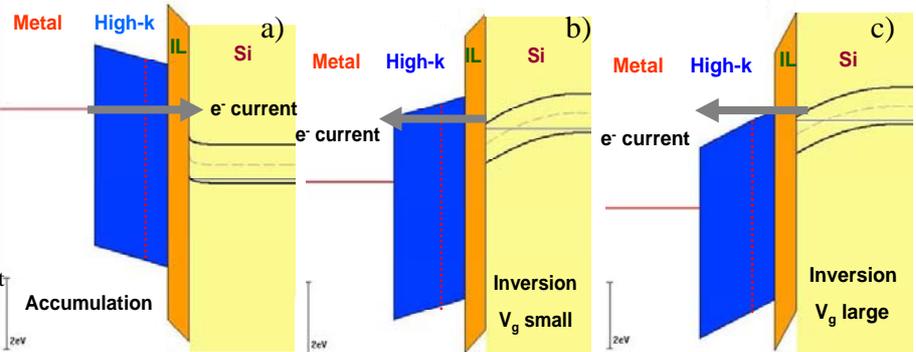


Fig. 10 The band diagram of the two-step dielectric stack under different gate bias conditions. In accumulation (a), as well as in inversion at low  $V_g$  (b), the electron transport proceeds through both high-k layers (the dotted line represents the interface between two high-k layers). In inversion under a high  $V_g$  condition (c), the electron current bypasses one of the high-k layers.

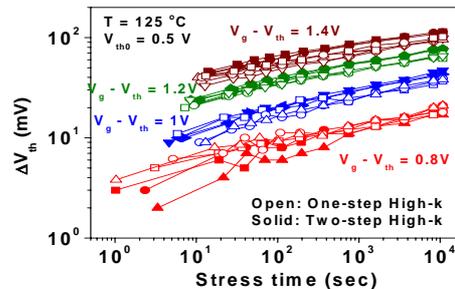


Fig. 11 Comparison of PBTI at 125 °C at different overdrive conditions for the one-step and two-step high-k devices.