Extended Abstracts of the 2010 International Conference on Solid State Devices and Materials, Tokyo, 2010, pp1036-1037

CVD Graphene for High Speed Electronics

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1. Introduction

Graphene, an atomically thin and hexagonal carbon layer, is a promising candidate as a material for post-silicon electronics. The major advantages of graphene are its 2-D structure and high intrinsic mobility. The 2-D structure makes it compatible with planar CMOS technology while maintaining much of the transport advantages of carbon nanotubes (CNTs). Graphene is also considered a very promising candidate for high-frequency devices due to its excellent electrical properties, such as a high intrinsic carrier mobility (> 10,000 cm^2Vs at room temperature) [1] and a large saturation velocity (~6–7 times higher than that for Si MOSFETs) [2]. A 100GHz GraFET has been demonstrated recently [3]. Several methods have been used for graphene synthesis, including: a) mechanical exfoliation of graphene from the surface of highly ordered pyrolytic graphite (HOPG) [4]; b) chemical exfoliation and stabilization of individual sheets in solution [5][6]; c) sublimation Si from single crystal SiC [7][8]; and d) Chemical Vapor Deposition (CVD) of graphene on the surface of single crystalline [9] or polycrystalline metals [10][11]. For VLSI applications, large-area graphene sheet on an insulator substrate should be a prerequisite. Among these approaches to synthesize a large scale graphene, CVD has been considered to be a promising approach for the manufacture of electronic devices. In particular, the use of Ni layer as a catalyst has been successfully demonstrated for the growth of large scale FLG (few-layer-graphene) [12] [13]. However, the growth behavior of graphene largely depends on Ni-catalyst layer, i.e., thickness, crystalline structure, surface morphology, chemical cleanliness, etc. Thus, in this work, we intensively studied the grain growth of Ni film and Ni dots and its subsequent growth conditions for obtaining SLG (single layer graphene) reproducibly. Finally, top-gated field effect transistors were fabricated out of the CVD grown graphene.

2. Graphene Growth

Graphene Growth on Ni Film

The substrate used for graphene growth was composed of 500nm polycrystalline nickel film deposited on SiO_2/Si substrates by electron-beam evaporator. It is believed that under high temperature, carbon is absorbed in nickel film. As the temperature goes down, the solubility of carbon in nickel decreases so that the carbon atoms segregate on the nickel surface and under certain circumstances, form graphene layers. One important factor to form FLG is the amount of carbon that was absorbed into the Ni-catalyst layer. It can be controlled by manipulating not only the amount of CH_4/H_2 gas ratio but also the cooling rate associated with the proper segregation of carbon for the formation of FLG.

The CVD growth of graphene in our study was carried out at a growth temperature of 880℃, with a pressure of 50 torr and a gas flow rate of 50 sccm of 5% diluted methane (CH_4) in argon (Ar) together with 500 sccm of H_2. The time for the growth varies from 50 seconds to 2 minutes. Post-growth cooling is carried out in a flow rate of 200sccm of Ar and 100sccm of H_2. Through the precise control of the annealing of Ni, growth and post-growth cooling down conditions, we could obtain ultrathin graphene film less than five layers on the Ni surface as presented in Figure 1.

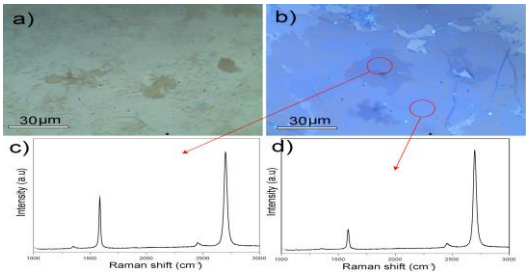

Figure 1. (a) Optical microscope image of the nickel surface after graphene growth. (b) Optical microscope image of the graphene transferred on the 90nm SiO_2 substrate. (c) and (d) Raman spectra of corresponding regions in (b). Raman measurements were conducted using a Rainshaw Raman system under λ_{exc}=632 nm laser excitation.

Graphene Growth on Ni Dots

For graphene grown on Ni film, usually one or two layers of graphene grow on top of the flat single-crystal grains and thick graphene layers are always observed at the grain boundary regions. By using a method to grow graphene on Ni dots with single or few grains, the total layers of graphene can be more precisely controlled.

500nm damascene Ni patterns in SiO_2 were annealed to achieve single or few grain Ni dots. Graphene was then grown on these few grain Ni dots by CVD. CH_4 gas was used as a precursor for carbon deposition at 900℃. After growth, graphene was transferred onto insulator substrate by wafer bonding and etch back technique. Optical microscope pictures of patterned graphene before and after transfer onto SiO_2 is shown in Figure 2(a), with Raman spectrum shown in 2(b). Under optical microscope, the

color of graphene patterns looks uniform. The Raman spectra shows negligible D peak compared with G peak. The 2D peak has a single Lorentzian profile and much higher intensity compared with the G peak. Roughly 60% of the patterns are single layer graphene. This transferred method shows zero misalignment, little contamination between the graphene and the substrate, and results in high transfer yields.

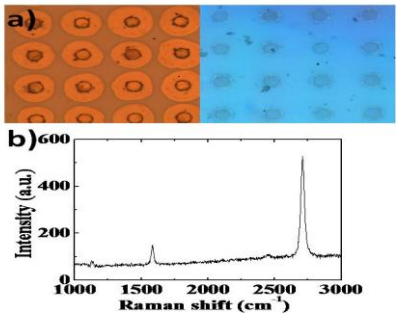

Figure 2. (a) OM Picture of Graphene grown on Ni dots and transferred on to SiO2 ~3μm patterns. (b) Raman spectrum indicates single layer graphene with good quality

3. Device Fabrication and Measurement

To fabricate the top-gated GraFETs with confined graphene channel, the graphene film was first patterned by photo lithography and oxygen plasma etching after PDMS stamping transferred to 100nm SiO_2 substrate. The transfer process is shown in Figure 3.

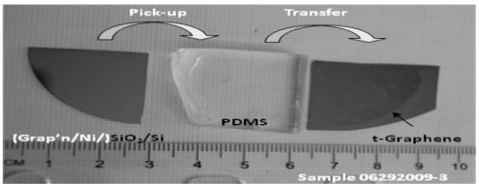

Figure 3. (a) Pick-up process: Attaching the PDMS with the CVD-grown Grap'n/Ni/SiO_2/Si and etching Ni/SiO_2 ($FeCl_3$ solution or HCl). (b) Transfer process: Putting the FLG/PDMS onto the 300nm SiO_2/Si substrate to transfer.

20nm Pd/30nm Au was then deposited on top of graphene as source and drain by e-beam evaporation. After that, 2nm Al was evaporated as a fuctionalization layer for dielectric deposition by atomic layer deposition (ALD). Before loading the samples from evaporator to ALD machine, the 2nm Al is believed to be quickly oxidized in the ambient [14]. 70 cycles Al_2O_3 was deposited by ALD as gate dielectric. The equivalent oxide thickness (EOT) of the 2nm evaporated Al and 70 cycles ALD Al_2O_3 is found to be around 7nm by ***C-V*** measurement. Following the gate dielectric deposition, 2nm Ti/30nm Au gate electrode was deposited, and patterned by lift-off. Finally, the Al_2O_3 was etched to open the source/drain contacts by diluted HF dip. The device structure is shown in Figure 4(a).

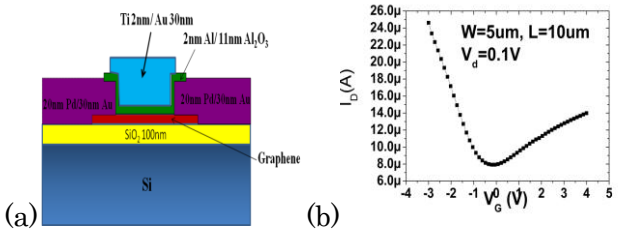

Figure 4. (a)A schematic of cross-section of a top-gated GraFET structure. (b) I_{DS}-V_{GS} characteristics of the top-gated GraFET.

Transistors were tested at room temperature and normal laboratory atmosphere. The DC characteristics of the top-gated GraFETs are shown in Figure 4(b). Figure 4(b) shows the drain current as a function of top-gate voltage $\boldsymbol{V_{GS}}$ at a drain bias of $\boldsymbol{V_{DS}}$=100 mV. The transfer characteristics exhibit the "V" shape behavior, reflecting the ambipolar transport in graphene. The Dirac point is at gate voltage about -0.4V. The low field FET mobility is estimated to be 500$cm^2 \cdot V^{-1} s^{-1}$ by transconductance method without subtracting contact resistance effect.

3. Conclusions

Graphene was successfully grown using chemical vapor deposition method on Ni film and Ni dots. Typical grain size of FLG grown on Ni film was several hundreds of μm^2. 60% of graphene sheets grown on Ni dots are single layer. Top-gated GraFETs were fabricated after the CVD grown graphene was transferred onto dielectric substrates. Ambipolar conduction was clearly observed, and the extracted mobility by transconductance method was found to be 500cm^2/Vs.

Acknowledgements

This project is funded by DARPA CERA program

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