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High Hole-Mobility 65nm Biaxially-Strained Ge-pFETs: Fabrication, Analysis and Optimization

J.Mitard, B.De Jaeger, G.Eneman[1,2], A.Dobbie[3], M.Myronov[3], M.Kobayashi[4], J.Geypen, H.Bender, B.Vincent, R.Krom[1], J.Franco[1], G.Winderickx, E.Vrancken, W.Vanherle, W.-E.Wang[6], J.Tseng[5], R.Loo, K.De Meyer[1], M.Caymax, L.Pantisano, D.R.Leadley[3], M.Meuris, P.P.Absil, S.Biesemans and T.Hoffmann

imec, [1]also K.U Leuven, ESAT-INSYS, [2]also FWO, [3]University of Warwick, [4]Stanford University, [5]TSMC, [6]assignee @imec. mitard@imec.be

1. Abstract: For the first time, high hole-mobility 65nm biaxially-strained Ge-pFETs, with reduced EOT while maintaining minimized SCE, have been fabricated and electrically characterized in-depth for the low and high field transport. The important role of pocket implants in drive current degradation is highlighted. Using a judicious implantation scheme, we demonstrate a significant I_{ON} gain (up to 35%) for nanoscaled strained Ge pFETs. Simultaneous optimization of metal gate and dielectric, together with the corresponding unixial stress engineering, is clearly the most promising path for further performance enhancement.

2. Introduction

New process modules (e.g. strain) and new materials are needed to keep improving transistor performance with scaling, especially for pFETs. However, most reported results that focus on [100] directed channels of strained-SiGe on relaxed (001) Si bulk substrates show a mobility reduction (hence drive current degradation) over the Si control in the short channel regime [1-3]. This effect was mainly attributed to Coulomb scattering and neutral defects due to junction implants [2]. While these defects in strained-SiGe pFETs seem a major showstopper for their final integration, this work will focus on *short channel strained-Ge devices* and present for the first time *a detailed analysis on the low and high field transport*. Finally, key parameters for further performance enhancement of strained Ge pFETs are given.

3. Substrate and Device Fabrication

200mm substrate fabrication starts from a (100) Si template and followed by a growth of a ~2µm-thick fully relaxed $Si_{20\%}Ge_{80\%}$ buffer and a 20nm-thick strained-Ge (s-Ge) layer grown by Reduced Pressure CVD [4] (fig.1). Defect etching reveals a threading dislocation density TDD ~$4x10^6$ cm^{-2} and an RMS surface roughness of ~2nm (fig.2). Moreover, the sGe channel layer doping was maintained at approximately 1E17cm^{-3} n-type in order to **1)** counteract the residual p-type defects after sGe growth, **2)** minimize junction leakage [5], and **3)** maintain a similar level of impurity scattering (dopants) between sGe and relaxed Ge pFETs (control wafers). The key device fabrication steps are summarized in fig.3. Gate stack and implants of these *bulk* devices are similar to devices reported in [6]. Finally, electrical measurements were carried out on regular structures (instead of ring-shaped ones [7,8]) to study a particular channel direction and to be as close as possible to manufactured devices. In addition, the low field mobility values for nanoscaled devices was corrected for R_{EXT} using the technique reported in [2,9].

4. Dielectric Properties and Substrate Quality Assessment

A TEM analysis of the 65nm biaxial compressive strained Ge pFET is shown in fig.4. The J_G-EOT_{INV} (fig.5) benchmark shows significant improvement in gate leakage mainly linked to the relatively thick Si/SiO_2 layers. The CET/EOT values in inversion (fig.6) around 1.9/1.45nm are among the best in class from literature results. Additional useful conclusions can be highlighted from fig. 6: **1)** similar doping level confirmed in the substrate, **2)** similar channel interface quality between relaxed and strained Ge devices, and **3)** slight increase of the band gap with strain (~0.15eV). Substrate quality was directly assessed with diode measurements and showed a factor of 20 reduction in leakage (fig.7). This appears to be consistent with the lower intrinsic carrier density in $Si_{0.2}Ge_{0.8}$ than for pure Ge ($n_{i,Ge}/n_{i,SiGe80\%}$~12 [10]) and possibly with a slight reduction in defects compared to bulk SiGe (the graded SiGe growth gives ~ one decade lower TDD than thick Epi-Ge layers). Finally, I_D-V_G and I_D-L_G traces (fig.8/9, respectively) show a good short channel effects control down to 65nm and an inversely-linear trend to the device scaling.

5. A Transport Study in Strained Ge pFETs

Similarly to strained SiGe devices [3], a significant improvement is observed in drive current for long channel 2D-strained Ge pFETs compared to relaxed ones (+70%) but the gain tends to disappear at short gate length (fig.9). This degradation is perfectly correlated to a net low field mobility reduction (fig.10) and hence to an increased impact of defects. *This result seems to confirm that strained-Ge and -SiGe pFETs suffer from a common transport-limiting mechanism.* To better understand this phenomenon, three different pocket implant conditions have been used and electrically characterized. As seen in HRTEM pictures (fig.11), the use of Arsenic halos (Process Of Record for relaxed Ge [6]) mainly gives twinning defects in the 20nm-thick strained-Ge layer while Phosphorus halos (at matched-activated dopants) give mainly dislocation defects. Note, no defects are seen in devices without pocket implants. The effect of these foregoing defects on low field transport is seen in fig.12 and clearly points to the critical role of halos in mobility degradation of short channels. For the first time, a substantial gain of I_{ON} for nanoscaled 2D-strained pFETs is demonstrated in Fig. 13 (up to 35% at 100nm). An extended analysis of the low field mobility at low temperature suggests that Coulomb scattering remains the main limiting mechanism in all short channel strained devices (fig.14). Finally, the velocity at the source is extracted (fig.15) and shows a strong increase when lowering the temperature even for the pocket-free strained device. This demonstrates that even after the careful attention to halo-induced defects yielding an improved performance for these sub-100 nm 2D-strained pFETs, the high field transport is velocity-saturation limited (i.e. diffusive) and so not purely ballistic.

6. Performance booster for 2D-strained pFETs

In addition to implant optimization, three improvement paths for both long and short channel sGe devices have clearly been identified as: **1)** lower doping in the strained layer (+7%) and optimized Si cap thickness/precursor [14] – fig.16 (+30%); (**2)** a metal gate electrode that does not counteract the existing compressive strain in the channel - using 10 nm TiN instead of 70 nm clearly improves the hole mobility (+12%) (fig.17 (expt.), fig.18 (simulation)); (**3)** employing longitudinal compressive stress or a transversal tensile stress, as demonstrated in fig.19.

7. Summary and Conclusions

65 nm 2D-strained Ge-pFETs have been successfully fabricated with an improved EOT_{inv} and control of short channel effects. The low and high field transport has been thoroughly investigated to identify the predominant role of pocket implants in reducing I_{ON} at short L_G. Further performance enhancement has been finally investigated: **1)** sGe passivation and channel doping, **2)** metal gate electrode, and **3)** Unixial stress. These optimizations will therefore allow the achievement of high-mobility channel Ge-pFETs with optimal switching speeds.

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References: [1] H.C,Wang, IEDM'04 [2] F.Andrieu VLSI'05 [3] W.-S Liao IEEE EDL 29, 2008. [4] M.Myronov, EMRS'09 [5] G. Eneman TED,55,8,2008 [6] J. Mitard IEDM'08 [7] A.Ritenour IEDM'03 [8] O.Weber IEDM'05 [9] D.Fleury. ICMTS'08 [10] F.Schaffler F. Eds. Levinshtein 2001 [11] S.W.Bedell EDL 29,7,2008 [12] Ghiani IEDM'03. [13] A. Lochtefeld, EDL, 22, 2, 2001. [14] J. Mitard VLSI'09

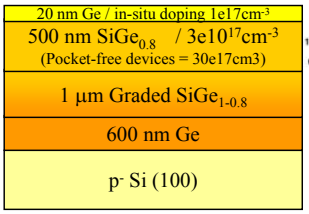

Fig.1: Schematic view of the substrate. The channel consists of a 20nm-thick biaxial compressive strained Ge layer. 500nm-thick $SiGe_{80\%}$ buffers are fully relaxed. *Note the SiGe doping was increased only for pocket-free devices (needed for SCE correction)*

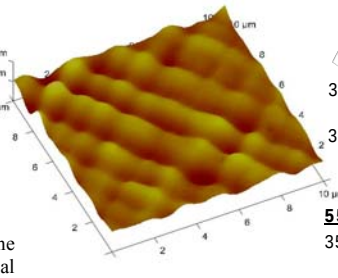

Fig.2: Surface morphology (AFM) of the SiGe virtual substrate after the Ge growth. The RMS roughness is found around 2nm.

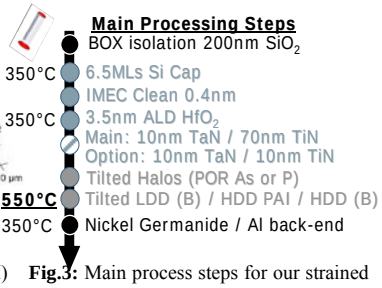

Fig.3: Main process steps for our strained and control Ge pFETs. The maximum thermal budget is limited to 550°C.

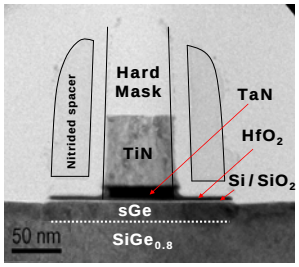

Fig.4: TEM images of a 65nm strained Ge pFETs using a 200mm Si compatible process flow.

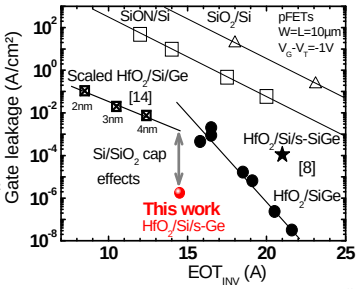

Fig.5: s-Ge pFETs J_G VS EOT_{INV} at fixed V_G-V_{TH} overdrive (-1V). Comparison with recent results in literature.

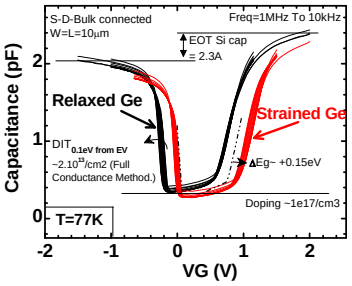

Fig.6: Full CV measurements at 77K showing the main electrical properties of the gate stack and substrate.

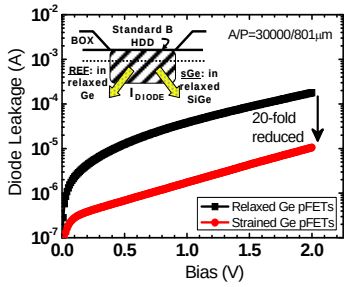

Fig.7: Reduced diode leakage for s-Ge/$SiGe_{80\%}$ structure compared to the reference (fully relaxed Ge pFETs)

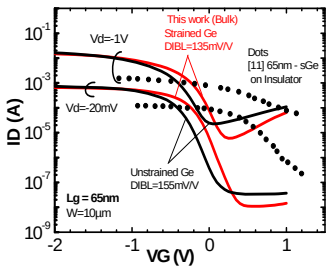

Fig.8: Full I_DV_G curves at low and high V_{DS}. DIBL is under control for our 65nm strained Ge pFETs.

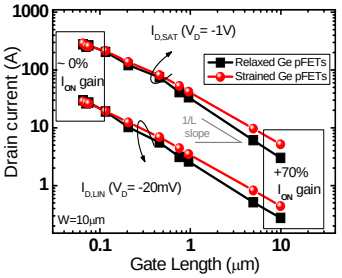

Fig.9: Drain current in s-Ge and r-Ge pFETs scales with L_G. At 65nm, similar, I_{DRIVE} is found in both linear and saturation regime.

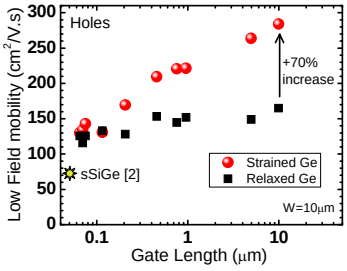

Fig.10: Low Field mobility corrected for R_{EXT} VS L_G. The I_{DRIVE} reduction seen in Fig.9 is correlated to a mobility drop.

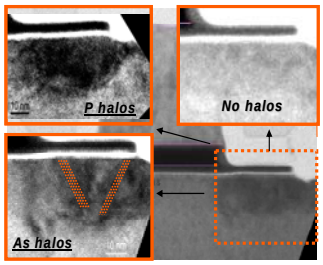

Fig.11: HRTEM pictures focusing on three different pocket implantation schemes TR) No halos TL) With Phosphorus (mainly dislocations) BL) With As (dislocations + twinning defects in the {111} plane)

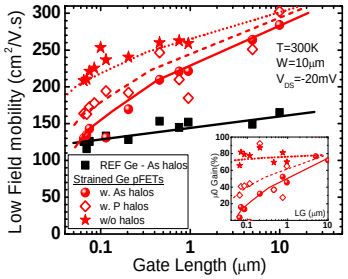

Fig.12: Impact of pocket implant schemes on low field mobility drop in the sGe technology. In inset, μ_0 gain from control Ge pFETs as a function of L_G.

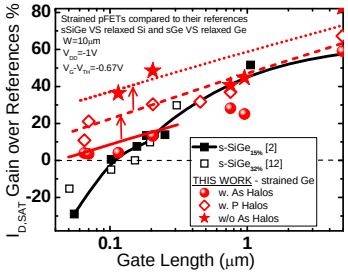

Fig.13: Pocket implants play a major role on $I_{D,SAT}$ gain in short channel strained Ge devices. Compared to sSiGe pFETs, a clear I_{ON} gain can be obtained.

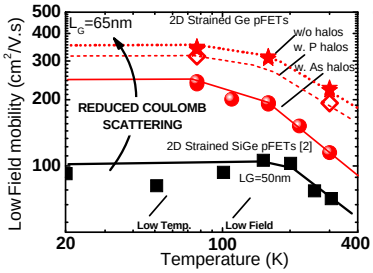

Fig.14: Low Field mobility VS Temperature. Coulomb scattering is clearly the limiting mechanism in all short 2D strained SiGe and Ge pFETs.

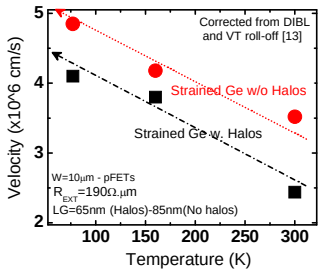

Fig.15: Velocity versus Temperature. The transport in our nanoscaled s-Ge pFETs seems to be diffusive rather than ballistic.

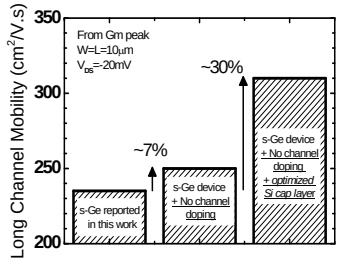

Fig.16: *Optimization 1*: Lowering the sGe doping and optimizing the Si cap passivation.

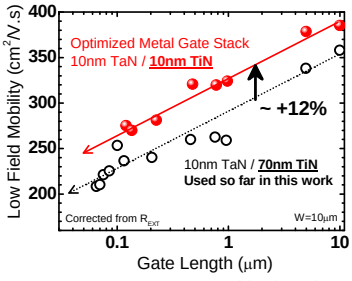

Fig.17: *Optimization 2*: Thinning down the intrinsically strained TiN. The existing 70nm TiN clearly reduces the stress component in the channel

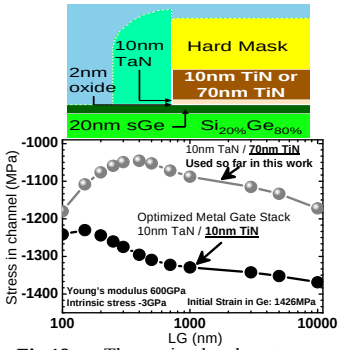

Fig.18: The simulated stress component confirms the experimental data shown in fig. 17.

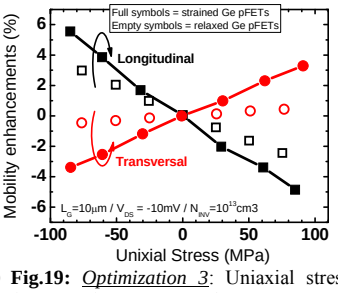

Fig.19: *Optimization 3*: Uniaxial stress for performance enhancement on strained-Ge. Comparison with relaxed-Ge pFETs. Measurements were done using a mechanical wafer bending set up.