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Ge FETs Gate Stack Passivation Options and their Scalability to low EOT

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1. Introduction

Due to its high intrinsic carrier mobility, Germanium is an attractive candidate for sub-22nm MOSFET technology, but it still remains difficult to be efficiently passivated. Recent reports claimed high carrier mobility for GeO_2-based MOSFETs [1-5] however at relaxed EOT. We report for the first time new understandings of the defects mechanisms occurring in GeO_2 scaled-EOT devices through modeling, physical and electrical characterization, in order to achieve high-mobility devices with low interface states density and low gate leakage current at relatively thin EOT (down to 0.65 nm).

2. Experimental

The GeO_2-based MOSFET devices presented in this study were fabricated using the process flow described in Fig. 1.

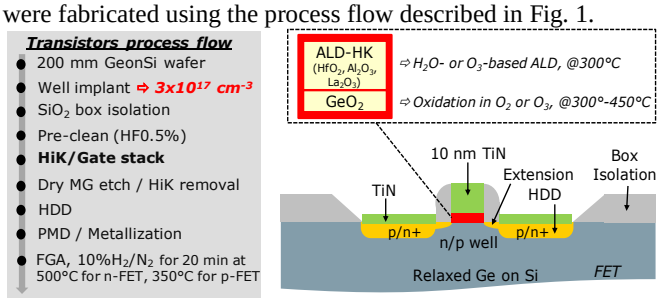

Fig. 1 *Process flow and schematic of Ge FETs devices*

3. Results and Discussion

Efficiency of GeO_2 IL growth on Ge substrate: The VT^2CP technique [6] allows profiling defects in both $Ge/Si/SiO_2/HfO_2$ and $Ge/GeO_2/HfO_2$ stacks (Fig. 2(b)). A higher trap density is found at the $Ge/Si_XGe_{(1-X)}/SiO_2$ interface, generated by Ge segregation [7] but also by the presence of Ge or Si dangling bonds (DB) at the $Ge_{(1-X)}Si_X/SiO_X$ interface - depending on the stress accumulated at this constrained interface (Fig. 2(a)). The GeO_2 visco-elastic properties result in a much reduced average stress at the interface [8]. Nevertheless, ab-initio calculation [9] predicts a Ge sub-oxides transition layer at the Ge/GeO_2 interface (Fig. 2(c)), leading to interface degradation.

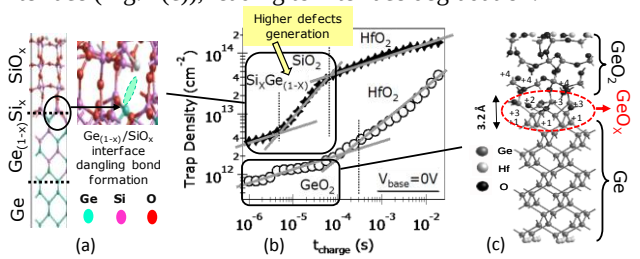

Fig. 2 (a) *Presence of Ge or Si DB at the $Si_XGe_{(1-x)}/SiO_X$ interface, explaining higher trap density in $Ge/Si/SiO_2/HfO_2$ stack observed in **(b)**; **(c)** Presence of Ge sub-oxides at the Ge/GeO_2 interface in $Ge/GeO_2/HfO_2$ stack.*

Impact of GeO_2 IL thickness and well doping reduction: Scaling down the GeO_2 IL generates more remote coulomb scattering defects and interface states promoted by a high fraction of sub-oxides at the Ge/GeO_2 interface (not obviously passivated), thus resulting in electron mobility degradation (Fig. 3(a)). Lowering the well doping from $3x10^{17}$ cm^{-3} to 10^{15} cm^{-3} reduces the coulomb scattering in the Ge channel, allowing 3.5x increase in peak mobility, resulting in 360 cm^2/Vs at a 3.6nm EOT for a $Ge/3.5nm\ GeO_2/4nm\ Al_2O_3$ stack (Fig. 3(b)).

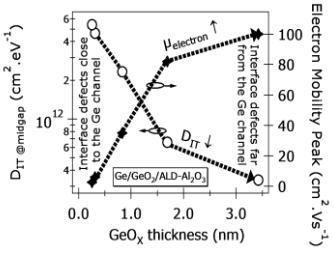

Fig. 3(a) *More interface traps for thinner GeO_2 IL leading to higher D_{it} and lower μ_e.*

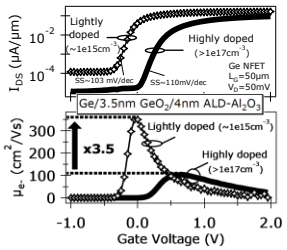

Fig. 3(b) *Lowering well doping reduces impurity scattering, leading to 3.5x mobility increase.*

Effect of HiK capping layer: In the GeO_X/HiK stack, large C-V hysteresis observed in Fig. 4(a) are indicative of the E_C and E_V band offsets at the interface which is insufficient to block e^- and h^+ injection leading to significant charge trapping in the stack [10]. Moreover, using the VT^2CP technique, D_{it} is found to be similar at the Ge/GeO_2 interface, but scanning further shows higher trap density at the GeO_X/HiK transition layer with HfO_2 compared to Al_2O_3 (Fig. 4(b)), further suggesting that the additional defects are metal-related. In agreement, ab-initio calculation [9] predicts a defect level presence at the $Ge/GeHfO_2$ interface due to a Ge-Hf bond formation, but a state-free $Ge/GeAlO_2$ (and $Ge/GeLaO_2$) interface as a result of Al incorporation into the GeO_2 matrix (Fig. 4(c)).

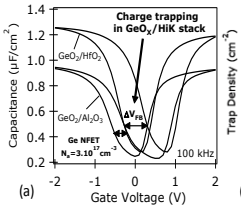

Fig. 4(a) *Large C-V hysteresis indicative of charge injection and trapping in the GeO_X/HiK stack.*

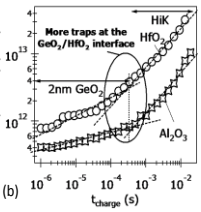

Fig. 4(b) *More traps when HfO_2 compared to Al_2O_3 suggesting metal induced defects.*

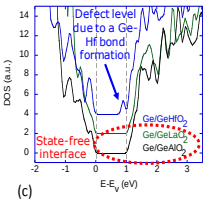

Fig. 4(c) *Defect level when HfO_2 due to Ge-Hf bond. No defect when Al_2O_3 thanks to a germanate formation.*

Use of La_2O_3 as alternative HiK for Ge passivation: La_2O_3 remains an attractive HiK thanks to its high-κ value (~25) and its ability to form aluminum germanate at the interface like Al_2O_3, as shown in Fig. 5(a). Both n- and p-FETs devices with a 4nm Al_2O_3/(1.2nm La_2O_3/)1.2nm GeO_2/Ge stack exhibit a relatively good I_{ON}/I_{OFF} ratio of 10^4-10^5 at V_D=±20mV and a low sub-threshold slope of ±85mV/dec, depending on the gate stack (Fig. 5(b)). Note that a lower amount of traps is found in the upper part of the Ge bandgap for the La_2O_3-based stack, as shown in Fig. 5(c). In agreement, La_2O_3 interlayer (IL) incorporation results in x3 times higher electron mobility enhancement. This observation further suggests an efficient Ge passivation by a germanate formation at the interface, promoted by the La_2O_3 IL. Moreover, replacing 4nm Al_2O_3 by 2nm HfO_2 on La_2O_3/GeO_2/Ge stack, allows EOT scaling from 3nm to 1.2nm, while maintaining the carrier mobility at ~75 cm^2/Vs.

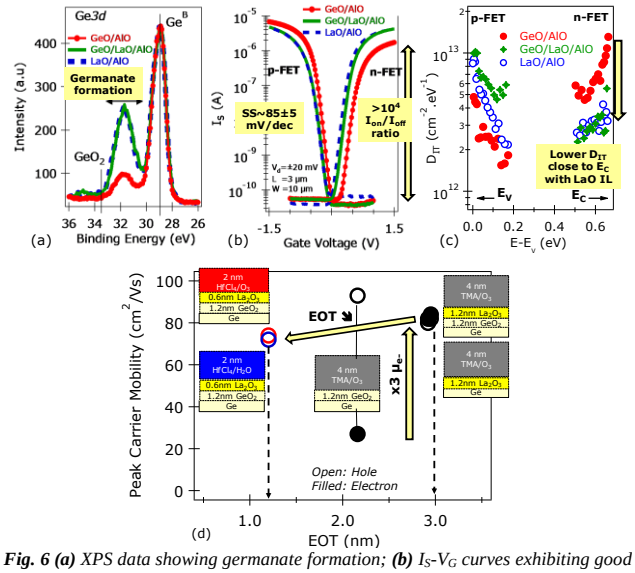

Fig. 6 (a) *XPS data showing germanate formation;* ***(b)*** *I_S-V_G curves exhibiting good SS and I_{ON}/I_{OFF} ratio;* ***(c)*** *D_{it} distribution within the Ge bandgap and* ***(d)*** *Peak mobility vs. EOT showing a 1.2nm EOT/ 74 cm^2/Vs μ_{h+} achievement.*

Impact of TiN MG on the interface: Further investigation on $Ge/GeO_2/La_2O_3/Al_2O_3$ stack reveal a GeO loss and ~40% Ge^{4+} oxidation states reduction after TiN deposition as shown in Fig. 7(a) and (b). TiN tends to adsorb the oxygen from the unstable GeO_2 IL through the HiK leading to interface degradation and a possible TiO_2 IL formation underneath TiN MG (Fig. 7(c)).

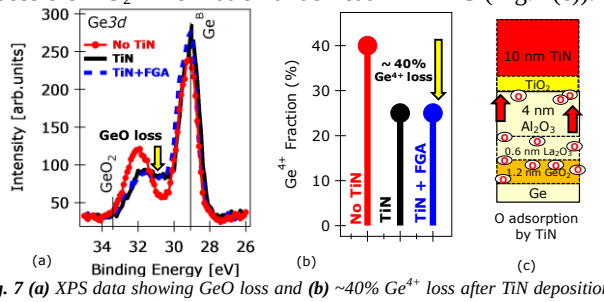

Fig. 7 (a) *XPS data showing GeO loss and* ***(b)*** *~40% Ge^{4+} loss after TiN deposition;* ***(c)*** *Schematic model of the O adsorption mechanism by TiN MG , resulting in interface degradation and TiO_2 IL formation.*

Use of HfO_2 HiK for EOT scalability: The use of La_2O_3 IL or/and Al_2O_3 as HiK impede aggressive EOT scaling. HfO_2-based stack could counteract this, allowing sub-nm EOT approach. As shown in Fig. 8(a) and (b), O_3-based ALD process results in thicker GeO_2 IL thickness, corresponding to a IL regrowth during the HiK deposition and exhibits a more pronounced GeO_2/HiK intermixing than H_2O-based ALD. GeO_2 IL can indeed be reduced by its interaction with water during the ALD process, due to its hygroscopic character.

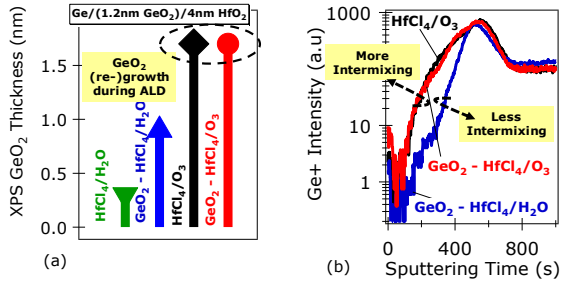

Fig. 8 (a) *Evidence of GeO_2 (re-)growth and* ***(b)*** *more pronounced GeO_X/HiK intermixing during O_3-based ALD process.*

As shown in Fig. 9(a), stacks using O_3-based ALD process exhibit a better SS~90mV/dec when 4nm HfO_2 is deposited on a thin GeO_2 IL or straight on Ge substrate, likely due to the IL regrowth during ALD (Fig. 8(a)). H_2O-based ALD devices exhibit a SS~163mV/dec (Fig. 9(a)) and high D_{it} values close to E_V side in Fig. 9(b), indicative of lower interface quality. Nevertheless, unlike O_3-based ALD devices which shows a high mobility (~95cm^2/Vs) but for a 1.5nm EOT, H_2O-based ALD process allows aggressive EOT scaling down to 0.65nm (Fig. 9(c)). This is the first known Ge MOSFET result reported so far at such low EOT, with conventional channel doping.

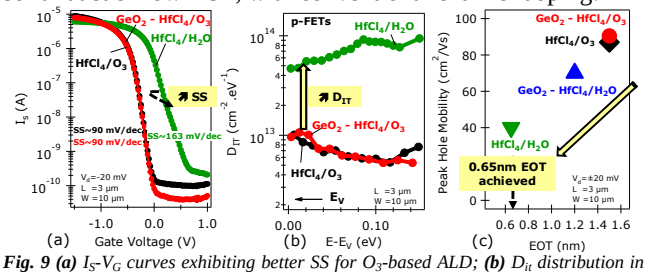

Fig. 9 (a) *I_S-V_G curves exhibiting better SS for O_3-based ALD;* ***(b)*** *D_{it} distribution in the Ge bandgap and* ***(c)*** *Peak mobility vs. EOT showing a 0.65nm EOT achievement.*

4. Benchmarking

A large gain of gate leakage current (10^1 – 10^3 reduction for J_G@ V_G-V_t= -1V) can be observed at relatively thin EOT with scaled GeO_2 interface in comparison to Si-based devices, as shown in Fig. 10(a). This observation suggests the ability of Ge-based devices to maintain a relatively low J_G at thin EOT. On the other hand, Fig. 10(b) presents peak electron mobility versus EOT benchmarking further pointing out the EOT-scaled range which reaches a low value of 0.65nm for the first time in Ge devices. Nevertheless, as the mobility drops with the EOT (like in Si devices), a Ge surface treatment prior to HiK deposition would be required to enhance the mobility.

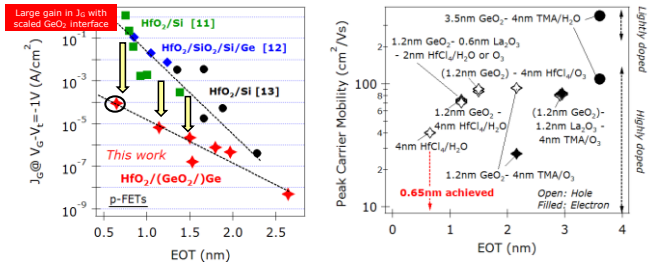

Fig. 10 (a) *J_G@V_G-V_t=-1V data exhibiting a large gain with Ge-based devices compared to Si one [11-13] at thin EOT;* ***(b)*** *Peak carrier mobility vs. EOT showing a 0.65nm low EOT achieved by a complete optimization of the gate stack.*

5. Conclusion

The mechanisms limiting the carrier mobility in Ge MOSFETs are comprehensively studied in low EOT region through the optimization of passivation layers, dielectrics, MGs, and doping conditions with in-depth electrical and physical analyses. By following the guidelines here, options for boosting mobility and reaching low EOT are proposed. A record 360 cm^2/Vs electron peak mobility at an EOT=3.6nm is thus demonstrated, corresponding to the best mobility on Ge n-FETs reported to date at such thin EOT. Moreover, a significant EOT reduction, 0.65 nm EOT, is achieved with a very low J_G~10^{-4}A/cm^2 (2 decades lower than that in Si devices). The potential of Ge-based devices in view of future sub-nm application is enlightened through this study.

References

[1] Nakakita, IEDM'08; [2] Kuzum, IEDM'08; [3] Saraswat, ECS'08; [4] Lee, ECS'08; [5] Lee, IEDM'09; [6] Zahid, IRPS'07; [7] Mitard, IEDM'08; [8] Houssa, APL **93**, 161909, 2008; [9] Houssa, APL **92**, 242101, 2008; [10] Afanas'ev, APL **92**, 022109, 2008; [11] Ragnarsson, VLSI'03; [12] Mitard, VLSI'09; [13] Weber, VLSI'04.