Extended Abstracts of the 2010 International Conference on Solid State Devices and Materials, Tokyo, 2010, pp1042-1043

Analysis of the Junctionless Transistor Architecture

Jean-Pierre Colinge[1], Jean-Pierre Raskin[2], Abhinav Kranti[1], Isabelle Ferain[1], Chi-Woo Lee[1], Nima Dehdashti Akhavan[1], Pedram Razavi[1], Ran Yan[1] and Ran Yu[1]

[1] Tyndall National Institute, University College Cork
Lee Maltings, Dyke Parade, Cork, Ireland
Phone: +353-21-490.4865 E-mail: jean-pierre.colinge@tyndall.ie
[2] Information and Communication Technologies, Electronics and Applied Mathematics
Université catholique de Louvain, 1348 Louvain-la-Neuve, Belgium

1. Introduction

The junctionless transistor is a heavily doped (several 10^{19} cm^{-3}) silicon nanowire with a multigate electrode. The doping concentration is constant throughout the device. There are, therefore, no doping concentration gradients, which greatly relaxes the processing thermal budget and facilitated the fabrication of ultrashort-channel and non-silicon devices [1]. Comparison of doping profiles in standard and junctionless devices is shown in Fig. 1.

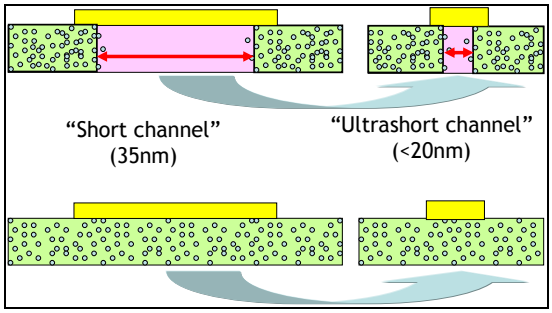

Fig. 1. Transistor with junctions (top) and junctionless transistor (bottom). The small "balls" represent doping atoms.

2. Mobility considerations

One might be concerned by the effect of the high channel doping concentration of junctionless gated resistors on carrier mobility. Electron mobility in silicon is shown in Fig. 2 as a function of donor concentration [2]. The mobility drops down to 80 cm^2/Vs for $N_D = 10^{19}$ cm^{-3} but does not significantly degrade any further as doping concentration is increased beyond 10^{19} cm^{-3}. A similar behavior is observed for holes in P-type doped silicon [2]. Channel mobility in inversion-mode devices is affected by the (vertical) electric field in the channel, E_{eff}. When EOT is reduced, surface channel mobility decreases, as shown for different technology nodes in Fig. 2 [3]. Mobility would now be well below 100 cm^2/Vs at the 45-nm node, if it was not for the introduction of strained silicon technology. The conduction channel in junctionless devices is in the center of the device, and that the electric field perpendicular to the current flow, E_{eff}, is very small. As a result, mobility in junctionless devices is not expected to decrease as EOT is scaled down [4]. Mobility in junctionless devices is largely dominated by ionized impurity scattering, and acoustic phonons seem to have little effect on mobility. As a result, the reduction of this mobility in junctionless devices with temperature (dμ/dT) is 5 times smaller than in regular devices with a lightly-doped channel [5].

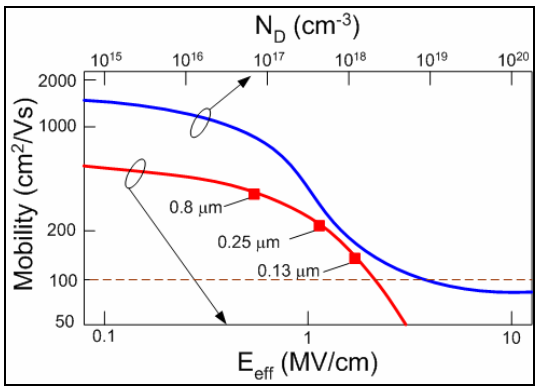

Fig. 2. Electron mobility in silicon as a function of donor doping atom concentration and as a function of electric field in the channel. The latter curve shows the mobility/field for several key technology nodes.

Since the channel of junctionless transistors is heavily doped, one might wonder if strain-induced mobility enhancement techniques can be effectively used in these devices. The devices were measured using a wafer probe system equipped with a 4-point bending setup that allows for bending the wafers in order to generate uniaxial strain in the transistors. The maximum stress is limited to 150 MPa to avoid breaking the wafers.

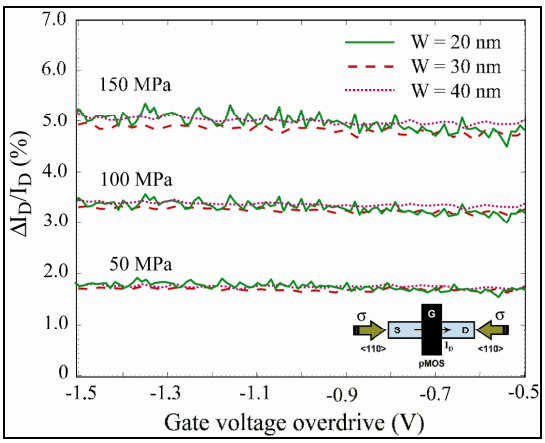

Fig. 3. Current variation as a function of gate voltage overdrive, V_{GS}-V_{TH}, in P-type junctionless devices under compressive stress.

The current increase induced by strain, $\Delta I_D/I_D$, was found to be linearly proportional to the applied strain and is in excellent agreement with theoretical values calculated for doped bulk silicon [6]. Furthermore, the mobility enhancement is independent of gate voltage, which supports the hypothesis of pure bulk transport (Fig. 3) [4].

3. Bulk Junctionless transistor

The feasibility of a bulk silicon version of the device was analyzed using 3D simulations. The cross-section of the N^+–N^+–N^+ device is 5×5 nm^2. The extension, *d*, of side gates into the moderately doped (10^{17} cm^{-3}) P–type region was optimized to control SCEs and leakage current. There is no lateral S/D junction along the current flow path, but a vertical PN junction is required for device isolation from the substrate. The gate is P^+ poly. It should be noted that a leakage current of ~ 30 pA and I_{ON}/I_{OFF}=3×10^5 can be achieved in the 10 nm bulk device (Fig. 6) and full device functionality is observed even in the absence of reversed biased lateral (source and drain) PN junctions.

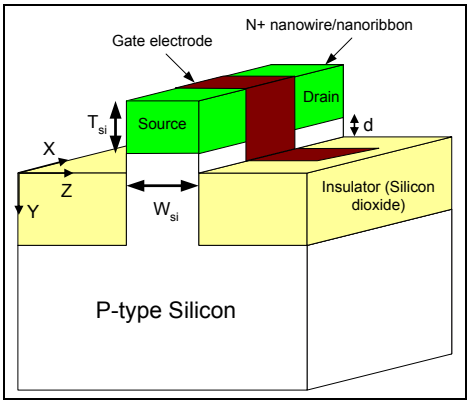

Fig. 5. Bulk version of the junctionless transistor.

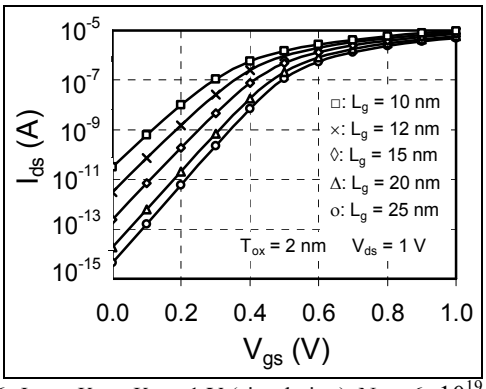

Fig. 6. I_D *vs.* V_G at V_{DS}= 1 V (simulation), $N_D = 6\times10^{19}$cm^{-3}.

Fig. 7 shows the cut-plane of the total current density through the middle of silicon channel at gate bias of 0.4 V. All current flow is through the N^+ region where the current density is the highest and not through the moderately doped P–type region or substrate. As the current flow is through the center of silicon film and not at the Si–SiO_2 interface, carriers observe a reduced electric field in the direction perpendicular to flow and carriers travel through the film with higher mobility which is much less influenced by surface roughness scattering as experienced by bulk inversion mode transistors, as in the case of the SOI device.

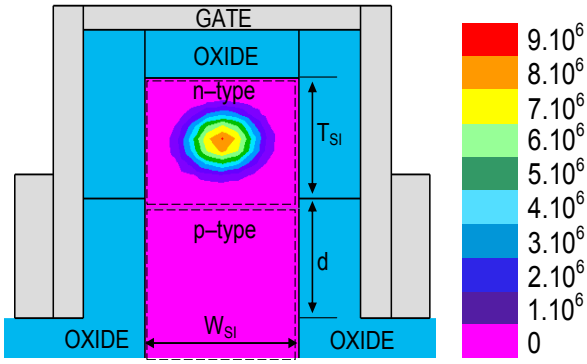

Fig. 7. 2D cut-plane showing the total current density distribution (A/cm^2) at V_{GS} = 0.4 V and V_{DS} = 50 mV (20 nm bulk device).

Fig. 8 shows the on-current as a function of device width and doping concentration, while adjusting the gate work-function to keep the off-current at 100 nA/µm. Increasing the junctionless device thickness from $T_{si} = W_{si}$ to $T_{si} = 2\times W_{si}$ increases the on-current by approximately 30%.

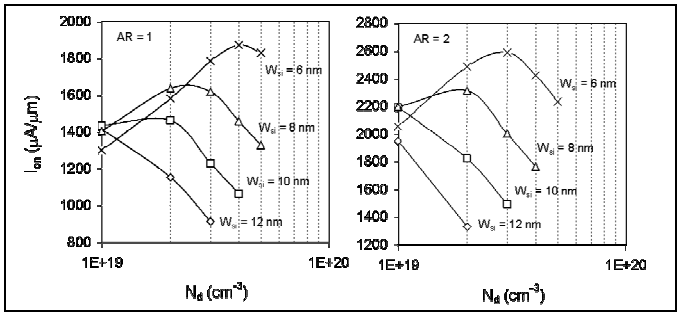

Fig. 8. I_D at $V_G = V_D$ = 1 V. Gate work function is adjusted to yield I_D = 100 nA/µm at V_G = 0 V and V_D = 1 V. Left: $T_{si} = W_{si}$; Right: $T_{si} = 2\times W_{si}$.

3. Conclusion

The issue of mobility in heavily doped junctionless silicon transistors is analyzed. The device enjoys bulk mobility and strain can be used as an effective means to improve mobility. The feasibility of a bulk silicon version of the device is studied by simulation, and performances similar to those of the SOI version of the device are obtained.

Acknowledgements

This work is supported by Science Foundation Ireland grant 05/IN/I888 and by the EC FP7 through the NANOSIL and EU-ROSOI+ Contracts 216171 and 216373.

References

[1] J.P. Colinge *et al.*, *Nature Nanotechnology* **5** (2010) 225-229
[2] C. Jacoboni *et al.*, *Solid State Electron.* **20** (1977) 77
[3] S.E. Thompson *et al.*, *IEEE TED* **50** (2004) 1790
[4] J.P. Colinge *et al.*, *Appl. Phys. Lett.* **96** (2010) 073510
[5] C.W. Lee *et al.*, *IEEE TED* **57** (2010) 620
[6] Y. Kanda, *IEEE TED* **29** (1982) 64