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Short-Channel Junctionless Nanowire Transistors

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1. Introduction

The junctionless transistor is a heavily doped (several 10^{19} cm^{-3}) silicon nanowire with a pi-gate electrode. In essence, the device is a normally-on gated resistor whose threshold voltage is positive because of the gate-to-nanowire work function difference [1]. So far, only long-channel devices (L=1μm) have been reported, but simulations predict that the junctionless transistor should have less short-channel effects than a transistor with junctions [2], and that gate lengths down to 3 nm should be achievable [3].

2. Device fabrication

Junctionless nanowire transistors with gate length down to 50 nm were fabricated using the process described in [1]. The gate oxide thickness is 5 nm and ebeam lithography was used to pattern both the nanowires and the gates. The n-channel devices were doped using arsenic to a channel concentration of $5x10^{19}cm^{-3}$ and P^+ polysilicon was used as gate material.

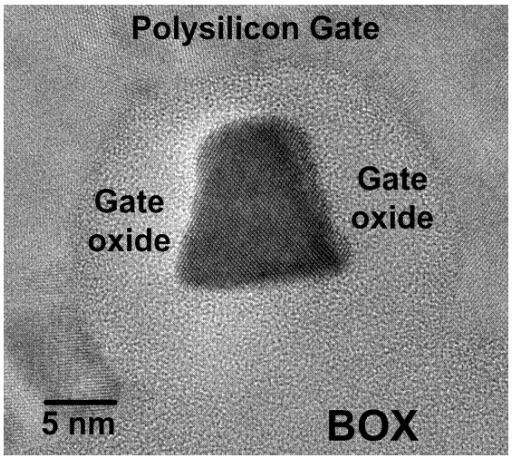

Fig. 1: Cross-sectional TEM picture of transistor showing the Π-gate (Ω-gate) structure of the device.

3. Short-channel effects

In MOSFET with junctions, part of the reduction of the threshold short-channel effects is due to the presence of a space-charge region associated with the junctions (*SCE* in equation below), and part of it (*DIBL*) is due to the growth of the drain space-charge region with drain voltage:

$$V_{TH} = V_{THO} - SCE - DIBL$$

where V_{TH0} is the long-channel threshold voltage [4,5]. In a MOSFET with physical gate length $L_{physical}$ (Figure 2c) the effective gate length is L_{eff} when the device is on, and the effective gate length is L_{SCE} when the device is off. Note that $L_{SCE}<L_{eff}$, which means that the "effective" channel length when the device is off is shorter than when it is on. In the junctionless transistor, the doping concentration is constant across the device. The electrostatic "squeezing" of the channel in the off device propagates into the source and drain; as a result, $L_{eff}>L_{physical}$ when the device is off (Figure 2a). When the device is on, the "squeezing" effect is removed, such that $L_{eff}=L_{physical}$ (Figure 2b). As a result, L_{eff} is larger on the off state than in the on state, which improves short-channel effects.

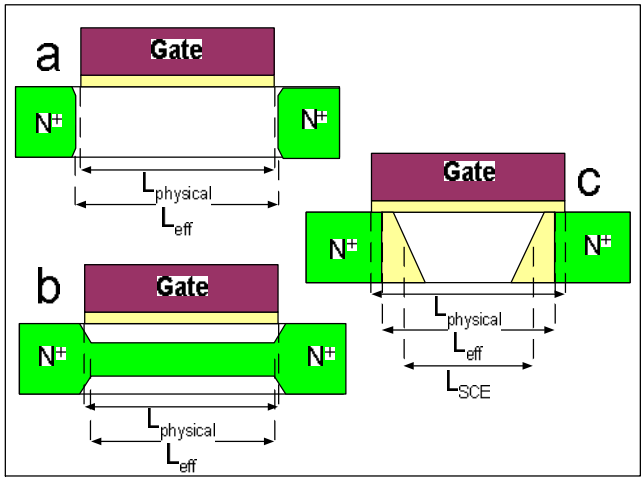

Fig. 2: Different effective gate lengths in a) a junctionless transistor in the off state, b) a junctionless transistor in the on state, c) an inversion-mode transistor.

4. Measurements

Drain current *vs.* gate voltage is shown in Figure 3 for a 50nm device. The short-channel effects are very low. The subthreshold slope ($SS = dV_G/d(log(I_D))$ at V_{DS}=1V is as low as 60 mV/dec for L=50 nm (Figure 4). The DIBL, defined as $V_{TH@Vds=50mV}$ - $V_{TH@Vds=1V}$ is equal to 7 mV for L=50 nm. These low values of DIBL are attributed to the absence of a drain junction. The blocking of current flow in the off state is not due to a reverse-biased drain junction but to "squeezing" off the carriers out of the channel region. When the device is off, the drain-source voltage drop occurs in the drain itself, and not in the channel region (under the gate) as in a regular device.[6] This dramatically reduc-

es DIBL.[2] The lack of channel length modulation by the drain is also visible in the output characteristics (Figure 5), which quite flat in saturation.

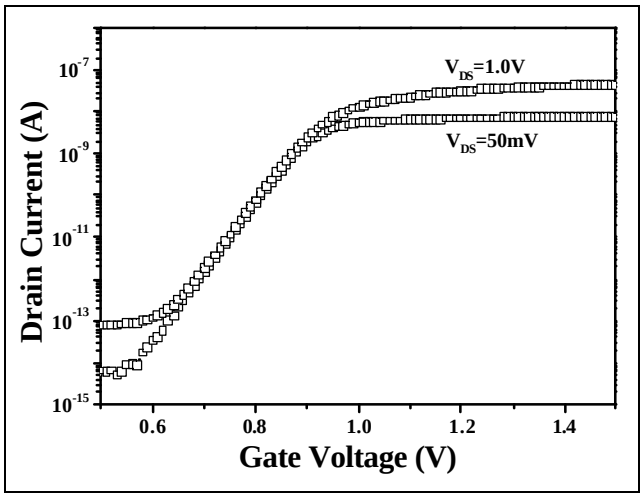

Fig. 3: Measured drain current *vs.* gate voltage in a 50nm device.

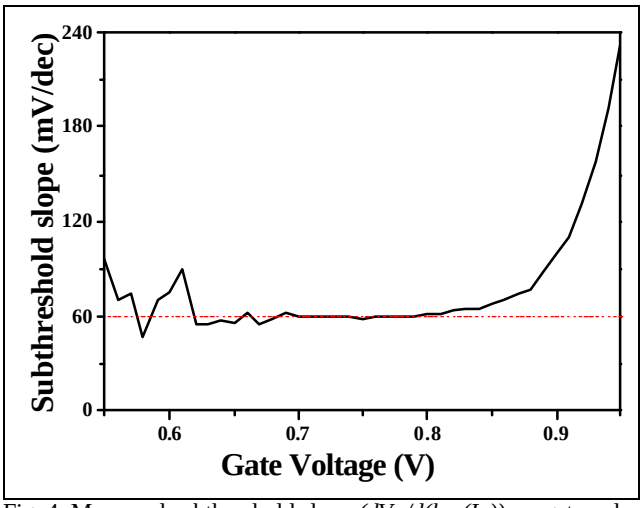

Fig. 4: Measured subthreshold slope $(dV_G/d(\log(I_D))$ *vs.* gate voltage in a 50nm device.

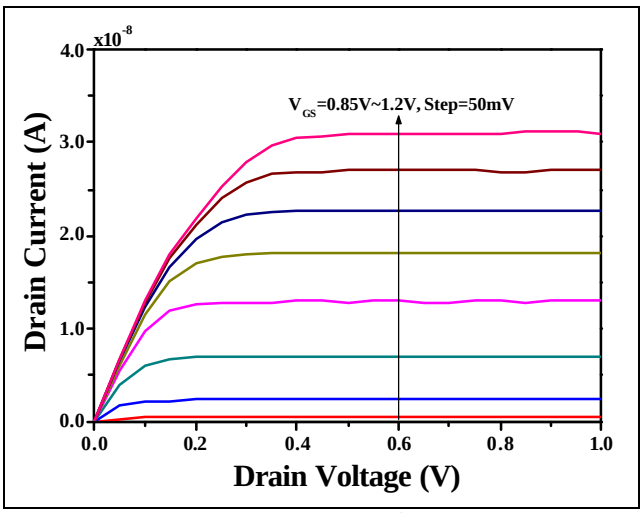

Fig. 5: Measured output characteristics of 50 nm-long n-channel device.

5. Discussion

Figure 6 shows the simulated electric field in an inversion-mode n-channel trigate FET (with junctions) and a junctionless transistor. Both devices are biased in the subthreshold regime with V_{DS}=1V and $V_G=V_{TH}$-200mV. As expected the peak electric field of the inversion-mode device is at the drain junction and the drain electric field extends to some distance in the channel region, contributing to both increasing DIBL and reducing the output impedance. In the junctionless device the region of high electric field is in the drain, outside of the region covered by the gate. It is wider than in the inversion-mode device, and the peak value is lower. As a result, the influence of the drain electric field on the channel region is much smaller than in the inversion-mode device, resulting in a smaller DIBL.

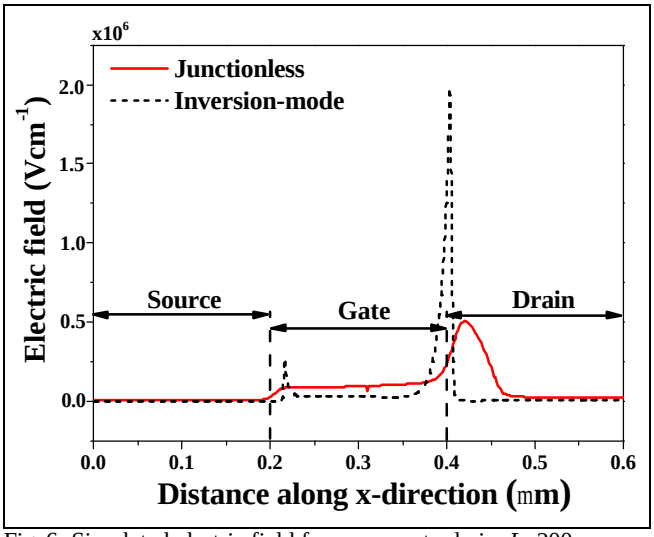

Fig. 6: Simulated electric field from source to drain. L=200nm, V_{DS}=1V. $V_G=V_{TH}$-200mV.

6. Conclusion

Junctionless silicon nanowire transistors with a gate length down to 50 nm have been demonstrated. The devices show very small short-channel effects: SS≅60mV/dec, DIBL=7mV.

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