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# Programmable optically reconfigurable gate array using a silver-halide holographic memory including six configuration contexts

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## I. Introduction

To date, optically reconfigurable gate arrays (ORGAs) have been developed to achieve both rapid reconfiguration and accommodation of numerous reconfiguration contexts [1]. The ORGA consists of a gate array VLSI, a holographic memory, and a laser diode array. The ORGA's gate array is reconfigured optically using diffraction patterns from the holographic memory, which is addressed using a laser diode array. Since such a holographic configuration enables parallel configuration using a massively parallel connection between the holographic memory and the gate array VLSI, ORGA architectures enable rapid reconfiguration. Moreover, since the storage capacity of a holographic memory is extremely large, ORGA architectures can provide numerous reconfiguration contexts or a huge virtual gate count that is much larger than those of currently available VLSIs. Consequently, ORGAs represent an alternative technology to the semiconductor technologies that are used currently.

Moreover, recently, a programmable optically reconfigurable gate array architecture has been proposed [2]. The architecture allows users to program it after it has been fabricated, as is true also for FPGAs [3][4]. However, to date, no practical demonstration using a non-volatile multi-context holographic memory device has ever been presented.

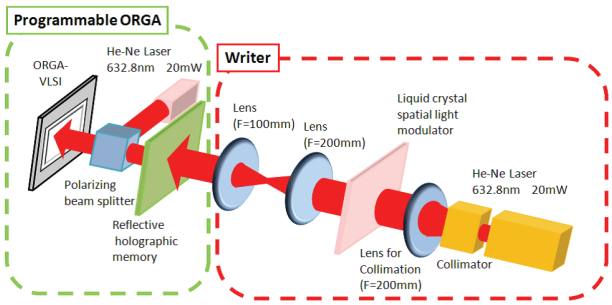
Therefore, this paper presents a practical demonstration of a programmable optically reconfigurable gate array (PORGA) using a silver-halide holographic memory including six configuration contexts. Aspects of the PORGA architecture performance were analyzed experimentally.

## II. Programmable ORGA

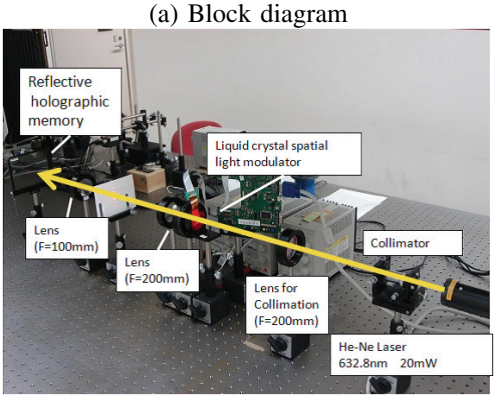
A block diagram depicting a programmable ORGA architecture and its writer is shown in Fig. 1(a). The right side is the writer part. The left side is the programmable ORGA part. The writer part comprises a collimated laser source and a liquid crystal spatial light modulator (LC-SLM). The programmable ORGA part comprises a laser array, a reflective non-volatile silver-halide holographic memory, and an ORGA-VLSI. First, a programmable gate array is set to a writer system, as shown in Fig. 1(a). Then, a configuration context is displayed on a liquid crystal spatial light modulator; a holographic memory pattern is recorded on a non-volatile silver-halide holographic memory on a programmable ORGA. The writer system can be removed once its holographic memory is recorded. Subsequently, the recorded programmable ORGA can work in standalone mode while numerous reconfigurations are executed.

## III. Experimental System

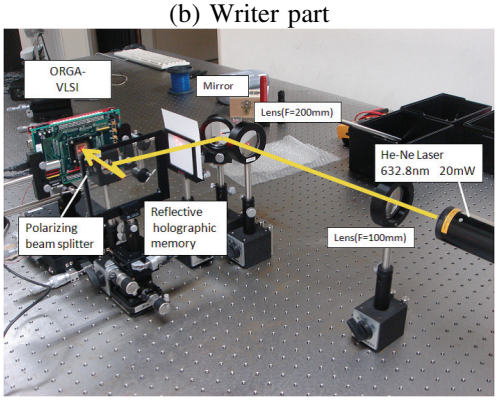
A constructed optical system is presented in Figs. 1(b) and 1)(c). The writer system was constructed using a liquid crystal spatial light modulator (LC-SLM) and a 632.8 nm He–Ne laser. The collimated laser beam is incident to the LC-SLM. The LC-SLM used to display a configuration context pattern, as presented in Fig. 2(a), is a projection TV panel (L3P07X-31G0; Seiko Epson Corp.), which is a twisted nematic device. The panel has 1,024 $\times$ 768 pixels, each having a size of 14 $\mu m$ $\times$ 14 $\mu m$. The LC-SLM is connected to the evaluation board (L3B07X-E10A; Seiko Epson Corp.). The board's video input is connected to the external display terminal of a personal computer. The diffraction pattern programming a silver-halide holographic memory was generated from the writer part. For the silver-halide holographic memory, PFG-01 silver film was used (Chuo Precision Industrial Co. Ltd.). The hologram material is 12.7 cm $\times$ 10 cm, but only a 7 mm $\times$ 4 mm area was used for this experiment, as depicted in Fig. 2(b). The hologram material coating thickness was 6–7 $\mu m$. The recording particles were smaller than 40 nm. For this experiment, the exposure time and power were, respectively, 240 s and 240 nW. A silver-halide holographic memory of programmable ORGAs was recorded using the holographic memory pattern beam from the writer. After programming, each configuration procedure can be executed by tuning the corresponding laser source, but in this experiment, only one laser was implemented because of limited hardware resources. Here, the light source for reconfiguration procedures on the programmable ORGA is also a collimated He–Ne laser. A polarizing beam splitter reflects the collimated beam, making it incident to the recorded silver-halide memory. Then, the reflected beam is incident to an ORGA-VLSI. The ORGA-VLSI was placed at a distance of 130 mm from the silver-halide holographic memory. The ORGA-VLSI was fabricated using a 0.35 $\mu m$ three-metal 4.9 mm $\times$ 4.9 mm CMOS process chip. In this fabrication, the




(a) Block diagram




(b) Writer part



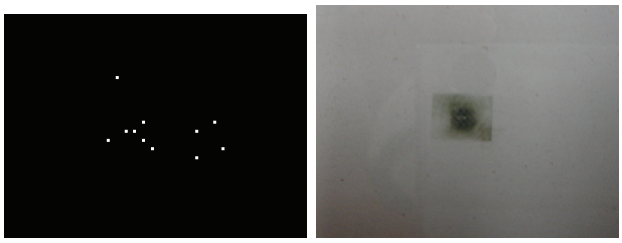

(c) Programmable ORGA part

Fig. 1. Block diagram and photographs of an experimental system.

distance between each photodiode was designated as 90 $\mu m$. Each of the 340 photodiodes is 25.5 $\mu m$ × 25.5 $\mu m$ to ease the optical alignment. The configuration context size is 20 × 17 bits. The gate array's gate count is 68.

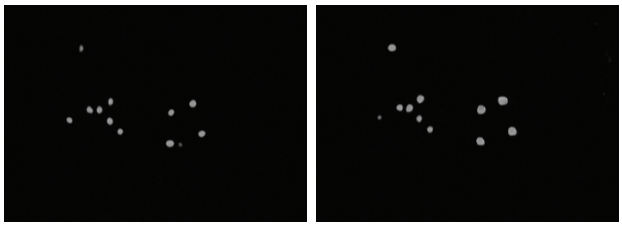
## IV. Experimental Results

In this experiment, an XOR circuit was programmed onto six recording regions on a silver-halide holographic memory of a programmable ORGA using the writer system to confirm a six-reconfiguration context capability. Each recording area of a silver-halide holographic memory is limited to a 2 mm × 2 mm area. A photofinishing process was then applied for the holographic memory. After being recorded, reconfiguration procedures for six regions were executed on a stand-alone programmable ORGA. Two samples of CCD captured configuration context patterns are shown in Figs. 3(a) and 3(b).



(a) (b)

Fig. 2. (a) Configuration context pattern and (b) a recorded silver-halide holographic memory of an XOR circuit.



(a) (b)

Fig. 3. CCD captured images of configuration contexts of XOR circuits generated from an upper middle side recording area and a lower right side recording area on a reflective holographic memory.

High-contrast configuration context patterns were confirmed. At that time, the reconfiguration times were measured as 9.5$\mu s$ – 26 $\mu s$, which is markedly faster than that of FPGAs.

## V. Conclusion

This paper has demonstrated practical application of a programmable optically reconfigurable gate array (PORGA) using a silver-halide holographic memory including six configuration contexts. Its programmability has been confirmed using a writer system. In addition, the reconfiguration periods were measured as 9.5 $\mu s$ – 26 $\mu s$. This experimental result presents the attractive possibility of development of a future ORGA that can accommodate more than 3,000 reconfiguration contexts on a 12.7 cm × 10 cm silver-halide holographic memory.

## VI. Acknowledgments

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## References

[1] J. Mumbru, G. Panotopoulos, D. Psaltis, X. An, F. Mok, S. Ay, S. Barna, and E. R. Fossum, "Optically Programmable Gate Array," Proc. SPIE - Int. Soc. Opt. Eng., vol. 4089, pp. 763–771, 2000.
[2] S. Kubota, M. Watanabe, "Programmable Optically Reconfigurable Gate Array Architecture and its writer," Applied Optics, Vol. 48, Iss. 2, pp. 302-308, 2009.
[3] Altera Corporation, "Altera Devices," http://www. altera.com.
[4] Xilinx Inc., "Xilinx Product Data Sheets," http://www. xilinx.com.