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Towards Optical Networks-on-Chip Using CMOS Compatible III-V/SOI Technology

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Abstract—**Integrated components for optical networks-on-chip, including III-V microdisk lasers, photodetectors, and wavelength selective circuits, are all demonstrated using a complementary metal-oxide-semiconductor (CMOS) compatible III-V/silicon-on-insulator integration technology at 200mm wafer scale.**

Keywords—silicon photonics; microdisk lasers and photodetectors; heterogeneous integration; network-on-chip

I. INTRODUCTION

Optical interconnects and more complex optical network-on-chip (ONoC) are likely to replace the current electrical wires for transporting information between processor cores [1]. However such architectures rely on the compliance of all photonic functions - including compact electrically injected laser sources - within silicon. Here we present our recent developments for future electro-photonic integrated circuits. In particular continuous wave operation microdisk lasers, photodetectors, and wavelength selective circuits are demonstrated using a CMOS compatible III-V/silicon technology at 200mm wafer scale.

II. CMOS COMPATIBLE INTEGRATION TECHNOLOGY

The integration scheme makes use of III-V semiconductor materials for both lasers and photodetectors, whereas passive circuits are realized by patterning silicon on insulator (SOI) films. A specific process adapting and modifying the standard III-V material process steps to comply with a CMOS environment is developed, using the so-called above-IC approach schematically represented in Fig.1. In this approach

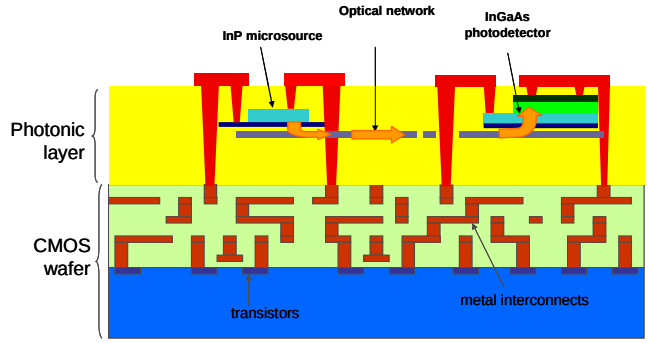

Figure 1. Above-IC silicon photonics and III-V/SOI integration scheme.

the devices are fabricated at the back-end of line (BEOL) levels keeping the temperature below 350°C. To achieve CMOS compatibility, i) die-to-wafer bonding was developed at the 200mm scale, ii) dry etching chemistry capable of etching the III-V dice while preserving the Si/SiO_2-based surface was investigated and iii) CMOS compatible metals were used to replace standard gold based contacts used in optoelectronics.

The heterogeneous integration of III-V materials and SOI circuits is performed with the die-to-wafer bonding technology; *i.e.* unpatterned III-V dice are integrated on top of a processed SOI wafer by means of SiO_2/SiO_2 direct bonding [2] This process under development allowed us to achieve a bonding yield in the order of 80% after complete InP substrate removal, as shown in Fig. 2a) and 2b).

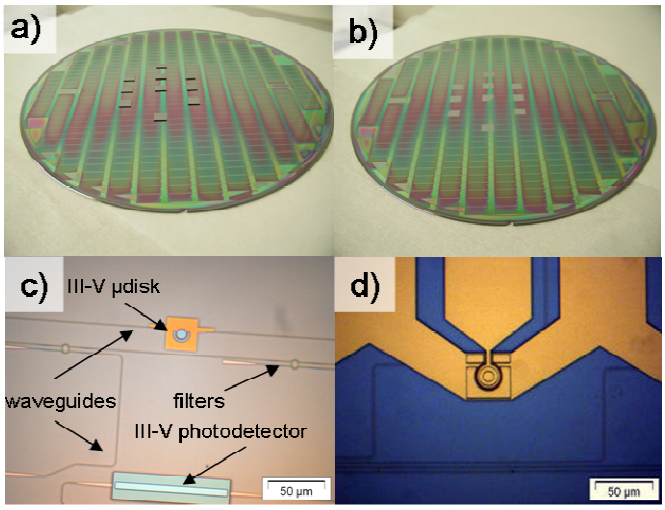

Figure 2: InP die-to-wafer SiO_2/SiO_2 direct bonding on 200mm passive optical circuits, (a) after bonding, and (b) after complete InP substrate removal.. Integration of III-V active devices on top of SOI passive circuits (c) after III-V dice etching and (d) after the metallization step.

An original III-V epi layer design where the laser and the photodetector heterostructures are stacked within the same epitaxy was implemented to fabricate the photonic chips (cf. Fig. 1). Compared to already demonstrated point-to-point links where some dice are dedicated to laser structures and some others to photodetectors structures [3], this enables a much more simple integration scheme as well as much lower footprint optical links. The total epitaxy thickness is only 1µm which enables the use of 248nm deep ultraviolet (DUV) lithography without focalization issues. The subsequent III-V processing, including wet and CH_4-H_2-based reactive ion etching, oxide isolation layer deposition, metallization, is optimized at 200mm wafer scale [4]. Figure 2c) shows an optical microscope image of both III-V microdisk laser [5] and photodetector on top of waveguides with a SiO_2 bonding layer thickness of 130nm. Regarding electrical contacts, the standard gold-based metallization and the usual lift-off technique to

define the contact area were discarded. Instead, a Ti/TiN/AlCu metal stack is deposited on the whole wafer. After a lithography step, the metal stack is dry-etched with a chlorine-based chemistry down to the oxide isolation layer which also acts as an etch-stop layer. Ohmic contacts on both n-InP and p-InGaAs are obtained without any annealing performed on the wafers [4]. Figure 2d) shows an image of a fully processed microdisk laser after contact metallization.

III. Microdisk Lasers, Photodetectors, and Thermally Tuned Ring Demultiplexers

Microdisk lasers with diameters of 20µm and 40µm were fabricated and characterized. The output power was collected at one end of the SOI waveguide by using a fiber grating coupler. Continuous-wave (CW) lasing at room temperature was observed. The light-current-voltage (LIV) curve of a 40µm diameter microdisk laser is shown in Fig. 3(a). The VI curve is similar to the one of devices fabricated earlier where gold contacts were used [6]. It can be seen that these devices have a threshold current of 6mA, corresponding to a threshold current density of 0.48kA/cm^2. A maximum output power of 150µW in the SOI waveguide was measured. The optical spectrum of such a microdisk laser at 23.4mA bias shows a side mode suppression ratio higher than 27dB (inset of Fig. 3a).

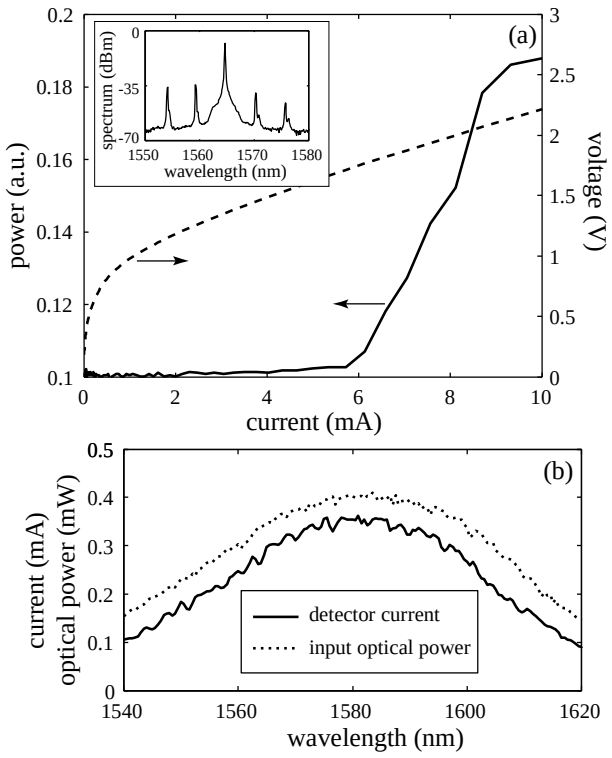

Figure 3. (a) LIV curve of a 40µm diameter microdisk laser. Inset shows the laser spectrum at 23.4mA bias. (b) Wavelength response of an evanescently coupled waveguide detector with an 80µm long absorption section.

Evanescently coupled waveguide detectors with various lengths were fabricated, and the SOI waveguides under the detectors were tapered to different widths to examine the coupling efficiency. Responsivity varies from 0.7A/W for detectors with 20µm long absorption sections to 0.9A/W for 100µm long absorption sections on top of 500nm wide waveguides. The wavelength response is shown in Fig. 3b) for a detector with an 80µm long absorption section. The Gaussian shaped spectrum is caused by the fiber grating couplers.

Wavelength division multiplexing (WDM) is necessary for improving the capacity of one connection. In ONoCs wavelengths can also be used as a routing mechanism between difference processor cores. Ring based (de)multiplexer is an ideal structure in this case regarding the footprint.

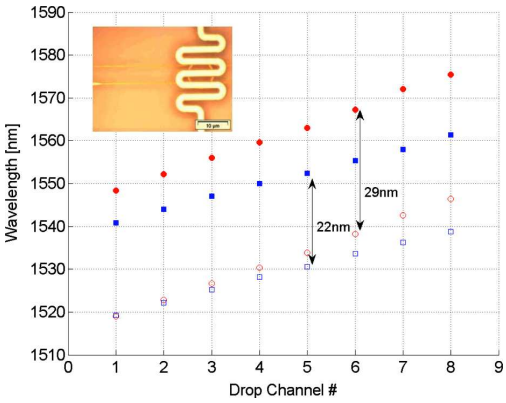

Figure 4. Experimentally measured channel wavelengths for two 8-channel demultiplexers with 29nm and 22nm FSR, respectively. The inset shows a microscope image of the fabricated heater with underlying ring resonator.

Figure 4 shows the measured channel wavelengths from two such demultiplexers. Each of them was built by cascading 8 SOI ring filters with slightly different diameters on one bus SOI waveguide. Uniform distribution of the channel wavelengths between one free spectral range (FSR) is presented. Further fine-tuning of the wavelength positions can be realized through an integrated Ti/TiN heater on top of each ring as shown in the inset of Fig. 4. A tuning rate of 0.3nm/mW was obtained experimentally [5].

IV. Conclusion

We have demonstrated for the first time a CMOS compatible III-V/SOI technology at 200mm wafer scale that enables the realization of microdisk lasers, photodetectors, and thermally tuned ring filters with promising performance, therefore paving the way to the demonstration of ONoCs.

V. Acknowledgment

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