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# Monolithic One-bit Counter Circuit with Light Emitting Diode Indicators Fabricated in Si/III-V-N/Si Heterostructure

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## 1. Introduction

Upgrading of information processing capability has been conducted by the miniaturization of Si-based LSIs. However, future miniaturization lead serious problems, such as heat management, increase of coupling noise and electromagnetic interaction between components of the circuits. To solve these problems, the concept of optoelectronic integrated circuits (OEICs) was proposed [1]. The monolithic integration of III-V-based photonic devices and Si-based LSIs is one of the ideal approaches for fabricating OEICs [2]. We have achieved individual operation of elemental light emitting diode (LED) and p-type metal-oxide-semiconductor field-effect transistor (p-MOSFET) on a single chip [3, 4].

In this report, we have fabricated a monolithic one-bit counter circuit with LED indicators in a lattice-matched Si/III-V-N/Si heterostructure. The fundamental properties of the circuits as well as the device characteristics were investigated.

## 2. Device Structure and Fabrication Process

The one-bit counter with LEDs was fabricated in a Si/GaPN/Si heterostructure [5]. A schematic diagram of the layer structure is shown in Fig. 1(a). This structure was grown on an n-type Si (100) substrate misoriented by 4° toward [011] direction using molecular beam epitaxy (MBE) system with two growth chambers [6-8]. A homo-junction of a 550-nm-thick n-GaPN and a 650-nm-thick p-GaPN for LED was covered with a 1.45-μm-thick n-Si capping layer for the fabrication of MOSFET. The cross-sectional image of the device is shown in Fig. 1(b).

The one-bit counter circuit consists of enhancement-enhancement (E-E) inverters and MOS switches. The logical value of input signal ($V_{in}$) and output signal ($V_{out}$) are displayed by GaPN LEDs, those are connected to the counter circuits by Al wiring.

Prior to the circuit fabrication, operation of the circuit was simulated by a simulation program with integrated circuit emphasis (SPICE) using model parameters of p-MOSFET, which was extracted from Si/III-V-N/Si heterostructure fabricated by our group. In the present circuit, a design of E-E inverter in n-Si capping layer is one of the key, together with the improvement of the quality of n-Si capping layer, such as reduction of residual impurities in the capping layer [8]. As a result of the simulation, the gate

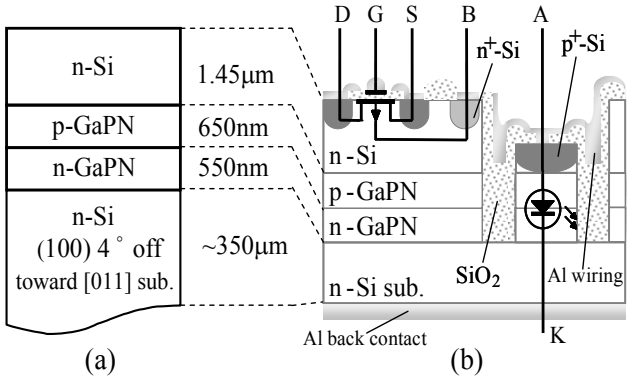


Fig. 1 Schematic images of (a) Si/GaPN/Si layer structure, and (b) cross section of p-MOSFET and LED fabricated in a Si/GaPN/Si heterostructure.

width and the length of p-MOSFET for the inverter circuits was designed to be 30 μm and 7 μm, respectively, namely W/L = 30/7. In order to reduce the occupied area of E-E inverter, we used 5 parallel p-MOSFETs in interdigital configuration [9], which is equivalent to single MOSFET of W/L = 150/7. To drive the present LED with area of 100 × 100 $\mu m^2$, 16 parallel p-MOSFETs were used to achieve the drive current up to 100 mA.

Fabrication process of the counter circuits with LEDs is based on the proposed methods for Si/III-V-N/Si heterostructures [6]. Device isolation was carried out by reactive ion etching (RIE) using $SF_6$ for Si, and $BCl_3$ for GaPN, respectively. Then a 1.2-μm-thick field $SiO_2$ layer was deposited by chemical vapor deposition. To increase an optical output, the Si capping layer on the LED region was etched to be 200-300 nm by RIE. This thin Si layer was doped with B by ion implantation to form $p^+$-Si contact layer. B and P ion implantation were carried out for source/drain and bulk contact, respectively. A 20-nm-thick gate oxide layer was grown at 900 °C for 10 min in wet $O_2$ ambient. A post-annealing after the ion implantation was carried out by the oxidation process. Finally, Al wiring and Ohmic contact formation were performed.

## 3. Results and Discussion

Figure 2 shows drain currents vs. drain voltages ($I_{DS}$-$V_{DS}$) and drain current vs. gate voltage ($I_{DS}$-$V_{GS}$) characteristics of the fabricated p-MOSFET. The threshold

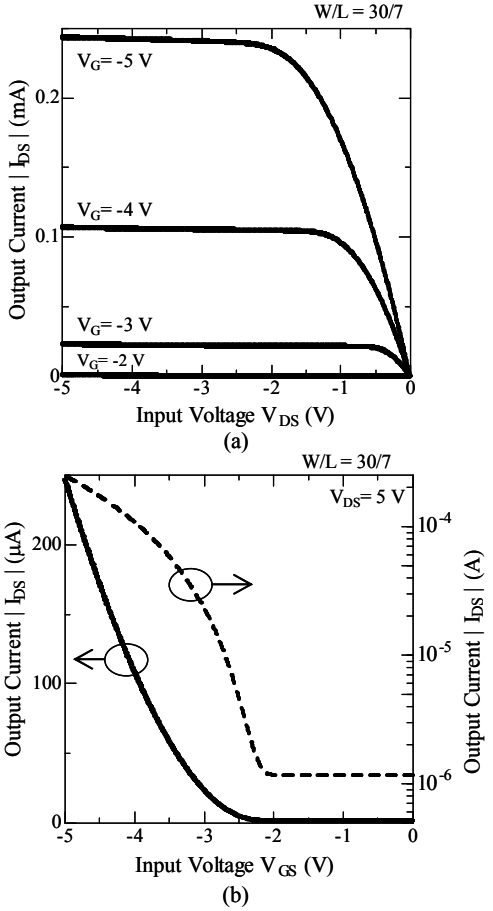


Fig. 2 Typical device characteristics of p-MOSFET. (a) $I_{DS}$-$V_{DS}$ characteristics with the $V_G$ changing from -5 to 0 V and (b) $I_{DS}$-$V_{GS}$ characteristics with the $V_{DS}$ = 5 V.

voltage of -2.1 V was obtained from $I_{DS}$-$V_{DS}$ characteristics. From SPICE simulation using this threshold voltage, operation of the counter circuit was confirmed. Figure 3(a) shows the chip micrograph of the fabricated one-bit counter circuits with LEDs in Si/GaPN/Si heterostructure.

The counter circuit was successfully operated with the driving voltage of 6.2 V, showing synchronized light emission from input and output indicators with the logical values of $V_{in}$ and $V_{out}$, respectively. The operation was confirmed up to the input frequency of 1 kHz. Further analysis, such as frequency response characteristics, is under way and latest data will be presented at the conference.

## 4. Conclusions

A monolithic one-bit counter circuit with LED indicator was fabricated, and its operation was successfully demonstrated. Present results suggest that our approach based on Si/III-V-N/Si heterostructure is promising for future OEICs.


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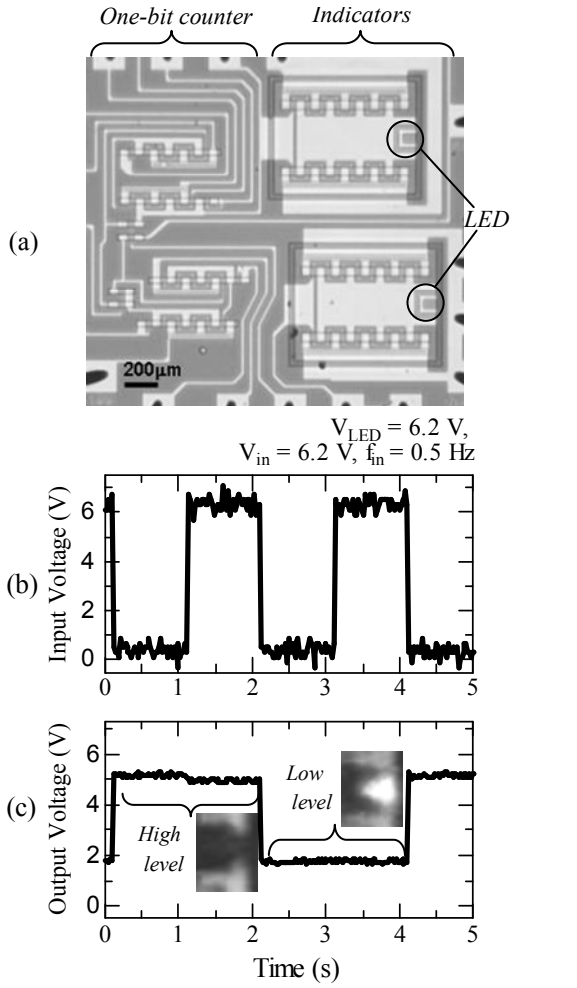


Fig. 3 Optical micrograph and device performance of one-bit counter circuits with LEDs. (a) micrograph of fabricated chip, (b) input voltage timing chart, and (c) output voltage timing chart with the snapshot of LED taken at 0.5 Hz.


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