Performance Improvement of a Novel Capacitor-less 1T-DRAM Based on a Lateral p Type Doped Region

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1. Introduction

For both scaling consideration and low process cost, floating body cells in SOI technology seem to be a promising candidate for the new generation of DRAM. All these new memory concepts are based on charging the body with the majority carriers generated by either impact ionization [1], gate-induced floating-body effect (GIDL) [2], intrinsic bipolar [3], or direct-tunneling current between partial n+ poly gate and n type silicon substrate [4]. Different types of architectures like Partially Depleted (PD) SOI, Fully Depleted (FD) SOI [5], FinFET [3], bulk silicon [6] have been studied. In this paper, we propose a new DRAM cell architecture using a highly p type doped lateral pocket localized in the p body silicon film of a PDSOI nMOSFET. This new architecture facilitates the formation of a deep body potential induced by impact ionization and single transistor latch. Therefore, a significant memory performance improvement measured on a standard SOI processing is demonstrated.

2. Memory cell characteristics

PD-SOI MOSFETs were fabricated in an industrial CMOS 65 nm SOI process provided by STMicroelectronics on conventional 300 mm Unibond® wafers with a 70 nm silicon film, a 5 nm gate oxide and a 145 nm buried oxide. These SOI MOSFETs were designed with three kinds of layout: 3-terminals for conventional device (1T-DRAM), Body Contacted (BC) device and specific layout to carry out a highly p doped Lateral Pocket 1T-DRAM (LP-1T-DRAM) localized in the p body silicon film (Fig. 1). No extra mask is needed to carry out this additional implant which is similar to pMOSFET source/drain ion implantation. The figure 2 shows typical output characteristics for the conventional 1T-DRAM, the BC device with grounded body and the new LP-1T-DRAM design. Body and source/drain architectures of these three devices are similar. Only the designs are different. The increase of drain current in the saturated current region of both the conventional device and the LP-1T-DRAM is due to the well known floating-body-effect caused by excessive hole accumulation created by impact ionization. The weak kink effect of the conventional 1T-DRAM becomes prominent with the novel architecture because the drain current is amplified by the parasitic bipolar effect. Indeed, in a first stage the excess of majority carriers tends to flow from drain to the highly p doped lateral pocket. Then as the drain voltage increases, the amount of excess holes is large enough to activate the parasitic BJT. Therefore, a large and abrupt increase of the

LP-1T-DRAM body potential in the saturation regime compared to the conventional 1T-DRAM is observed (Fig. 3). These characteristics prove that both conventional and new design devices can be used as memory cell by sensing the difference of drain current level after creating or removing the holes in the body. Contrary to parasitic BJT write and read conditions used to activate bipolar action in accumulation regime [7], the impact ionization write conditions with only one pulse generator connected to the drain, are easy to implement with LP-1T-DRAM. The optimal read current margin is obtained with the back gate grounded which illustrates the partially depleted feature of these devices. After write "1" and write "0" operations, a $125\mu A/\mu m$ large difference between the source currents for "1" and "0" states was measured at 25°C for LP-1T-DRAM (Fig. 4). This sensing margin is 5 times higher compared to the conventional design due to the high amount of charge stored in the body region. The sensing margin improvement observed with LP-1T-DRAM at 25°C is confirmed at 85°C (Fig. 5). Experimental results show a retention time of one second for the LP-1T-DRAM at 85°C (Fig. 6). This retention time, which is defined as the time it takes to close the read current difference by 50%, increases by almost a factor 50 compared to the conventional approach. The figure 7 summarizes the latest results published on capacitor-less DRAM using various writing mechanisms. The BJT writing operation with specific source/drain [9-10] provides better performances in terms of sensing margin and retention time than impact ionization. However the performances measured on the novel LP-1T-DRAM concept with easily implemented applied voltage and conventional source/drain engineering are in line with the best results obtained with BJT writing operation and specific source/drain.

3. Conclusion

A novel architecture based on a highly p type doped lateral pocket was proposed on a PD SOI device. Due to the single transistor latch, the body potential was significantly enhanced with this new design. Thanks to this feature, a new concept of capacitor-less 1T-DRAM with performance improvement has been demonstrated with conventional junction engineering. This novel 1T-DRAM provides a design solution to more effectively store holes. Therefore, large sensing margin (Δ Is=110µA/µm) and long retention time (1 second) at 85°C have been achieved. This device which needs neither an extra mask nor an additional process step and a single pulse generator, is a promising candidate for future high performance embedded 1T-DRAM.

References

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Fig. 1 (a) Schematic top layout and cross-sectional view from line A-A of the LP-1T-DRAM device (b) BC device (c) 1T-DRAM.



Fig. 2 Id(Vd) characteristics at Vg=1.4V for conventional 1T-DRAM, LP-1T-DRAM and BC device. Lg=140 nm.



Fig. 3 Vbody(Vd) characteristics at Vg=1.4V for conventional 1T-DRAM and LP-1T-DRAM devices. Lg=140 nm.



Fig. 4 Measured source current time dependencies of conventional 1T-DRAM and LP-1T-DRAM devices at 25°C. Lg=140 nm.



Fig. 5 Measured source current time dependencies of conventional 1T-DRAM and LP-1T-DRAM devices at 85°C. Lg=140 nm.



Fig. 6 Read current behavior of data 1 and data 0 of conventional 1T-DRAM (blue line) and LP-1T-DRAM (red line) devices as a function of hold time at 85° C. Lg=140 nm.



Fig. 7 Comparison of 1T-DRAM sensing margin as a function of retention time for various work and writing methods with usual 85°C.