Characterization of junctionless Z-RAM cell

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1. Introduction
Scaling down DRAM cell size to the nanometer regime poses several problems such as short-channel effects, leakage currents, complicated capacitor formation process and shallow junction formation. The Multigate FETs (MuGFETs) are very promising devices for nanoscale integration due to better short junction formation. The Multigate FETs (MuGFETs) are very used to realize a 1T DRAM, based on measured electrical characteristics and on simulations.

2. Device Fabrication and simulation
The 3-dimensional schematic view and cross-sectional transmission electron microscopy (TEM) image of fabricated JL FETs are shown in Figs 1 and 2, respectively. The devices were fabricated on standard Unibond SOI wafers with a 340nm top silicon layer and a 400nm buried oxide. The SOI layer was thinned down to 10-15nm and patterned into silicon nanowire using e-beam lithography. A 10nm gate oxide was grown using dry oxidation and arsenic ion implantation was used to dope the silicon nanowire uniformly N⁺ with a concentration of 1-2×10¹⁹ cm⁻³ to realize N-channel JL devices. P⁺ polysilicon was used as gate material. A gate length (Lgate) of 1µm was used in this work. Fig. 3 compares the structure of JL and IM n-channel devices.

3. Results and Discussion
Fig. 4 shows the operation mechanism of the JL Z-RAM (zero-capacitor RAM) device. The operation principle with a JL structure is same as in an inversion-mode (IM) device which used floating body effect. Impact ionization near the drain junction produces electron-hole pairs. The generated holes increase the potential of the transistor body in the channel region, which in turn decreases threshold voltage and increases the drain current. The increase of current increases the impact ionization rate, which completes a positive-feedback loop. Fig. 5 shows the measured drain current vs. drain voltage in JL and IM MuGFETs with forward and reverse V_D sweep and VGS=VTH-0.4V. The hysteresis cycle is used to distinguish a “0” from a “1” state after writing under low or high drain voltage, respectively. The turn-on voltage (V_on) of the JL MuGFET is much lower than the IM device due to the higher impact ionization rate in JL MuGFETs [5], with implications for low-power, low-voltage programming. The sensing window of JL MuGFETs is smaller than that of IM MuGFETs due to the lack of a P-type region in the channel of JL MuGFETs. However the sensing margin of JL MuGFETs is almost same as that of IM MuGFETs. A high V_on is needed because of the long channel. Fig. 6 shows I_D-V_D characteristics in simulated JL and IM short-channel double-gate devices. In short-channel device V_on is reduced due to the higher impact ionization rate and higher gain. Fig. 7 shows the electron concentration and hole concentration in the JL device of Fig. 6. One can see the electron and hole concentration suddenly increase at latch-up voltage due to the positive feedback effect. Fig. 8 shows typical I_D(V_G) curves of JL FETs (15-parallel devices). Fig. 9 shows the measured I_D(V_G) of JL FETs. The measured retention time for best device is close to 15s at room temperature (Fig. 10). Retention time decreases at higher temperature as shown in Fig. 11. Fig. 12 shows the source current during the programming has and illustrates the good programming window.

3. Conclusions
We fabricated the silicon nanowire JL proposed for capacitorless 1T DRAM. The JL-MuGFET has more advantage such as a very low leakage current, a low turn-on voltage, extremely easy processing. We believe that this JL based Z-RAM memory will use in sub-nano scale regime.

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References
Fig. 1: 3-dimensional schematic view of the junctionless MuGFETs device.

Fig. 2: cross-sectional high-resolution TEM photograph along A-A’ direction in fig.1.

Fig. 3 Schematic view of junctionless and inversion-mode n-channel devices.

Fig. 4: cross-sectional schematics of possible causes of latch-up in JL double-gate devices.

Fig. 5: Measured drain current hysteresis characteristics of JL and IM MuGFETs with $V_{GS}=V_{DD}=0.4\text{V}$ (single nanowire).

Fig. 6: Simulated $I_D-V_D$ characteristics of JL and IM double-gate device with $L_{gate}=100\text{nm}, T_{sl}=10\text{nm}, T_{ox}=2\text{nm}$.

Fig. 7 Simulated electron concentration and hole concentration in JL double-gate device at center of channel from top-gate to bottom-gate for different drain voltage values.

Fig. 8 Measured $I_D(V_D)$ of 15-nanowire JL MuGFETs with $W_{max}=50\text{nm}$ and $L_{gate}=1\text{um}$.

Fig. 9 Measured $I_D-V_D$ characteristics of the JL MuGFETs device at different gate voltages.

Fig. 10: Measured retention characteristics of the JL MuGFETs device at room temperature.

Fig. 11: Measured retention characteristics of the JL MuGFETs device at 85°C.

Figure 12 – Measured source current during cell operation for JL MuGFETs device with $W_{max}=50\text{nm}$ and $L_{gate}=1\text{um}$. 