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A Study of a Data Retention Characteristic for Various Schemes of Gate Oxide Formation in Sub-50 nm Saddle-Fin Transistor DRAM Technology

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Abstract

A data retention characteristic has been investigated for different gate oxide formation schemes with Saddleï Fin (S-Fin) transistor DRAM. The interface traps strongly affected the data retention time which was not clearly understood with Gate-Induced-Drain-Leakage (GIDL) current. Despite the lower GIDL current by the thicker side-wall oxide of a dry oxidation scheme than a radical scheme, the degradation of the retention time was originated from the high interface-trap-density (D_{it}). It is worthwhile to note that the D_{it} is a still significant parameter to analyze the tail distribution of the data retention time.

Introduction

A Saddle-Fin (S-Fin) configuration has a much attraction as a DRAM cell transistor due to its high gate controllability and extended effective-gate-length. However, the S-Fin DRAM was not much investigated due to its complicated structure and process steps. Nevertheless, it was confirmed that the main data loss mechanism which determines the DRAM data retention is a Gate-Induced-Drain-Leakage (GIDL) current which is one of major storage-node leakage components for a recessed channel structural transistor as shown in Fig. 1 [1,2]. The GIDL leakage has strong dependency on gate oxide thickness. Thus, we looked into the data retention characteristics for the different gate oxide (GOX) formation schemes such as dry oxidation which provides a partially thickened oxide profile due to its silicon orientation dependency and radical oxidation of excellent conformality through monitoring the GIDL current and interface-trap-density (D_{it}) by a charge pumping test [3,4].

Experimental

Figure 2 shows a process flow for the body-tied S-Fin transistor. It initially starts with (100) p-type bulk Si wafer. After the silicon active patterning, the line type etch is non-selectively performed and selective oxide etch was followed to make a recess fin structure. Finally, a n^+-doped polycrystalline silicon was deposited and a gate was formed through a dry-etch. This flow is summarized in Fig. 3. Fig. 4 and its inset depict the cross sectional TEM images of the S-Fin FinFET and the bird eyeôs view 3D schematic in the y side of Fig. 2(c). As afore-mentioned, the gate oxide was split to 6 different recipe and schemes as summarized in Table. 1.

Results and Discussions

When targeting the bottom oxide thickness, a dry scheme makes the thicker side oxide where the junction-to-gate is overlapped than a radical oxide case, due to the silicon orientation dependency of thermal oxidation as depicted in Fig. 5. For splits, their thicknesses were ordered as follows: split1(dry)>split2>split3>split4>split5(radical) as shown in Fig. 6.

Figure 7 shows the GIDL current dependency on the threshold voltage (V_t). The high dry GOX potion caused the relatively high V_t and low GIDL current due to its thick side wall GOX. Fig. 8 represents the median GIDL current of 74 points for each split. It was expected that the dry oxide would guarantee the enhanced data retention due to its thick GOX. However, the split5(radical) tied the longest and the GIDL current did not explain the data retention behavior properly in Fig. 9. To address the retention behavior, the charge pumping test was approached to estimate an energy distribution of interface states which is a main cause to govern the leaky cells, as shown in Fig. 10. The highest D_{it} was attained with the dry GOX. The results, ordered in a number of D_{it}, were as follows: split1(dry)>split2> split5(radical)>split3>split4. Considering the WF-to-WF variation, the dry GOX induced a higher D_{it} than a radical one in this experimental. The D_{it} well reflects the data retention behavior for the GOX formation splits except for the one deviated point which has the low GIDL current level. It was confirmed that the GIDL current cannot represent the D_{it} fully. Thus, both monitoring of the GIDL current and D_{it} will be a right direction to manage the tail distribution of the data retention. Furthermore, it has been reported that as a DRAM technology shrinks down to a nanoscale, the tail distribution of the data retention time will be separated with main one [5]. But, that phenomenon was not clearly appeared in this sub-50nm regime.

Conclusions

To sum up, we investigated the GOX dependency on the DRAM retention characteristics. Despite the higher GIDL current of the radical scheme, it has a better retention characteristic than the dry one. It was identified that the GIDL current is not the only parameter to govern the tail distribution of the data retention. Also, the D_{it} by the charge pumping test is still meaningful parameter to keep tracking in terms of the management of DRAM data retention.

References

[1] S. Park, *et. al.*, in *Proc. 46th Annu. IRPS*, 2008. [2] T. Hamamoto, *et. al.*, IEEE Trans. Electron Devices, vol. 45, no. 6, pp. 1300, 1998. [3] M. Chang, *et. al.*, *IEEE Trans. Electron Devices*, vol. 52, no. 4, pp. 484, 2005. [4] G. Groeseneken, *et. al.*, *IEEE Trans. Electron Devices*, vol. ED-31, pp. 42, 1984. [5] K. Kim, *et. al.*, *IEEE Electron Device Lett.*, vol. 30, No. 8, pp. 846, 2009.

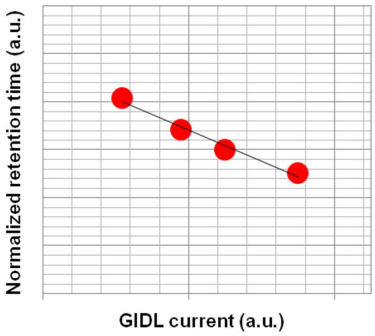

Fig. 1 DRAM retention characteristic of S-Fin FinFET on GIDL current.

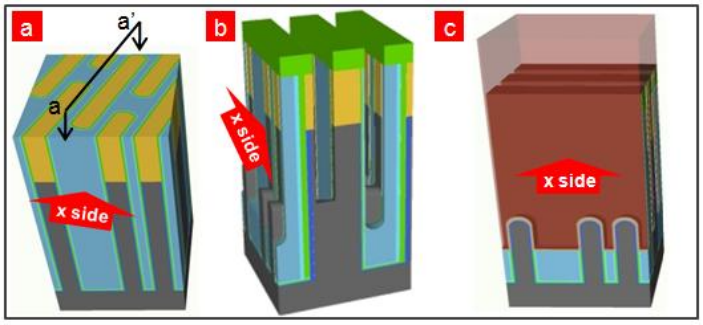

Fig.2 3D schematic of S-Fin transistor fabrication after (a) STI formation, (b) silicon etch and STI recess, and (c) gate formation.

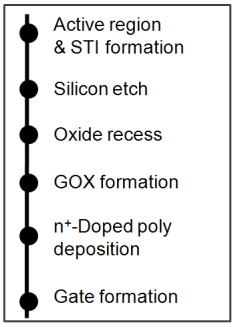

Fig. 3 Process flow of S-Fin FinFET.

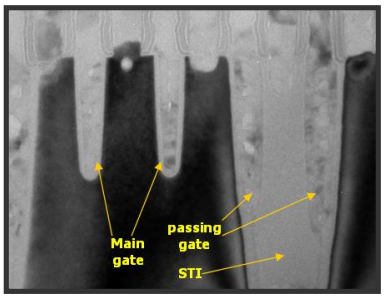

Fig. 4 Cross section TEM image along a-aô direction in Fig. 2(a). The inset depicts a birdôs eye view of the 3D schematic in y side of Fig. 2(c).

Split	Condition
1	Dry
2	
3	Increased Dry GOX portion
4	
5	Radical

Table.1 Summary table for GOX split conditions

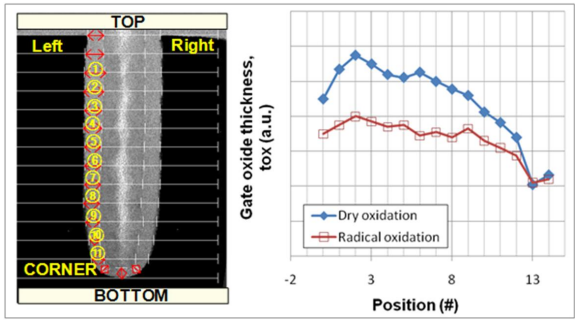

Fig. 5 Cross section TEM image over the recess region after the gate oxide formation & the gate oxide thickness along the positions for the two dry and radical schemes.

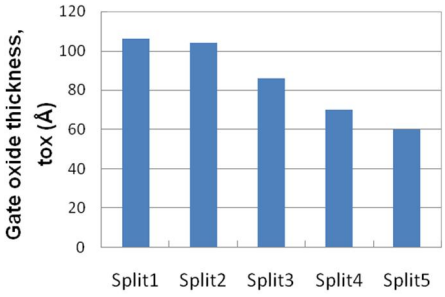

Fig. 6 The gate oxide thickness trends for all splits on the same spot in the side wall of the recessed silicon..

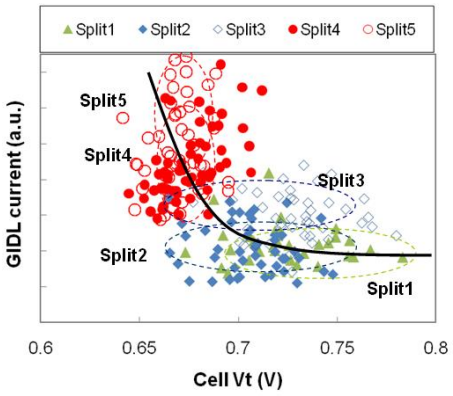

Fig. 7 GIDL current dependency on the cell transistor V_T for every gate oxide formation schemes.

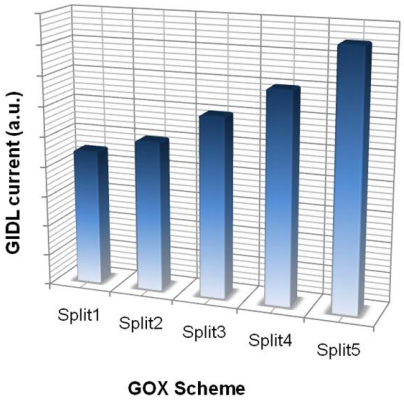

Fig.8 A median GIDL current trend for 74 points of each GOX split.

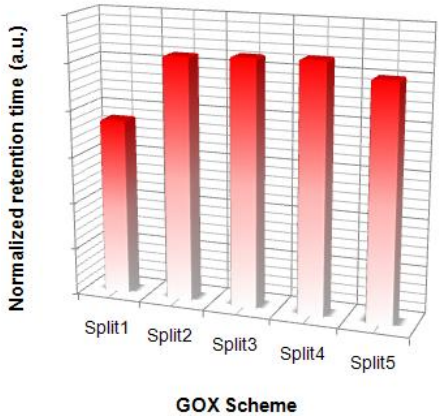

Fig. 9 The normalized data retention time characteristics for the different GOX formation schemes.

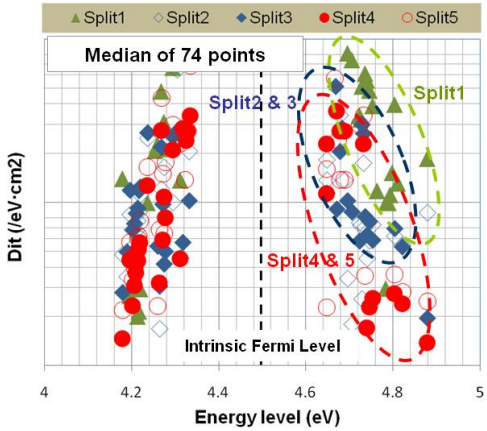

Fig. 10. The extracted D_{it} along energy level. Dry oxidation shows the highest shallow-level- interface-trap density.

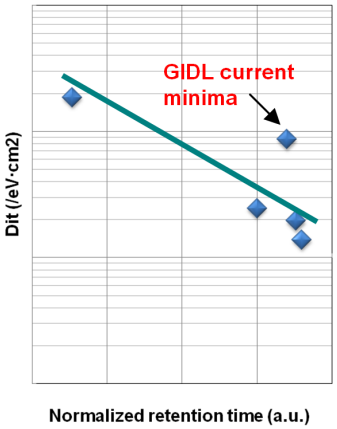

Fig. 11 The summarized D_{it} dependency on the data retention time.