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E-2-1

Improvement of Data Retention in NAND Flash Memory for beyond 3x nm using HTO Liner and IPD Thickness Optimization

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Abstract

As cell size shrinks in NAND Flash memory, assuring adequate reliability characteristics is getting difficult due to the sensitivity of Flash cell against small process changes. Especially, it is still unclear how the combination of mechanical stresses encapsulating the cell structure affects the reliability characteristics. In this paper, we present our results on how to improve reliability with optimizing mechanical stress in active and interpoly dielectrics (IPD) thickness, and confirmed the results through various simulations and test methods on 41nm NAND technology. Hereafter, we need to fully confirm the ISO and IPD beyond 3x nm technology node.

1. Introduction

Fig.1 shows the stored electron number and tolerance of charge loss in the FG cell, which is evaluated as a function of technology node. As the technology scales down, reliability becomes a major concern due to the decrease of stored electrons and tolerable electron loss number. Generally, improvement in reliability had been accessed from the viewpoint of dielectric quality such as Tox and ONO [1-3]. Also the PSZ material in sub 50nm technology is essentially used due to the provision of better ISO gap-fill margin. But the PSZ material has the demerit point in that it experienced shrinkage after ISO processing thereby affecting the mechanical stress at the active area. In this paper, we will review the liner material adopted in STI process and ONO thickness. In addition, the mechanical stress of liner material and mechanism of charge loss are discussed.

2. Results and Discussion

As shown in Fig.2, the simulation showed mechanical stress in the channel direction of a memory cell. The mechanical stresses varying across the different position along the channel are indicated in Fig.2 (a). Generally over 50nm technology has compressive mechanical stress due to HDP material gap-fill. But sub 50nm technology has tensile stress by PSZ volume shrink. This stress was mainly induced during wafer processing such as liner deposition or ISO PSZ gap-fill after STI process. At the center region, tensile stress of HTO liner was lower by around 7% as compared to LPTEOS liner. Interface trap density was evaluated by using high/low frequency capacitance method, which is more sensitive for monitoring of the traps at and near the Si/SiO2 interface. Charge trapping has been attributed to both interface and bulk traps. HTO liner deposition after wall oxidation showed lower interface trap density, lower electron charge trapping and this could probably be due to the mechanical stress being lower than conventional liner (Fig.3 and Fig.4). In other words, we can improve charge trapping with less tensile stress liner material. The cell distribution after high temperature bake, had been improved in the case of HTO liner as illustrated in Fig.5. It showed that the interface trap recovery and electron de-trapping are the major mechanisms, while stress induced leakage current (SILC) does not play such a big part. Fig.6 shows the stress simulation for HTO liner thickness. As the HTO liner thickness increased, the tensile stress in the channel was suppressed by the PSZ volume decrease. And the bake shift is directly proportional to the tensile stress. It is evident that the stress relaxation in the channel is a major factor of interface trap generation. Using these experimental items, retainability of data improved during high temperature bake with mechanical stress free. The schematic plot of possible leakage current path is shown in Fig.7. Stored electrons in FG move out from bottom oxide to inter-nitride layer. Then these electrons moved to the adjacent cell. In order to confirm this mechanism, Low Temperature Data Retention (LTDR) was used for the evaluation and simulation for pattern dependency. The results showed that the worst pattern is column bar (Fig.8 and Fig.9). In the BL to BL potential, it was correlated with charge loss of programmed cell. This means that the major mechanism of charge loss is due to the difference in potential in the BL direction. Fig.11 shows Raw Bit Error Rate (RBER) versus bake time for ONO split. Compared to the conventional ONO structure at 3-week LTDR, a thicker ONO3 case revealed a little improvement but still failed, while a thicker ONO1 can showed much improvement of about 2-order in RBER and passed the LTDR specification (<1E-4 at 1year) because of suppressing electron traps to nitride layer.

3. Conclusion

To improve reliability, we propose a use of HTO material as a liner and thicker bottom oxide for ONO structure. It is demonstrated a big improvement for HTDR and LTDR in data retention characteristics. Also, we provide a guideline for ISO liner and ONO structure in NAND Flash cells through TCAD simulation and measurement.

References

[1] Yohwan Koh, IMW, pp.1-3, April 2009.
[2] Akio Toda, et al., IRPS, pp.250-256, 2005.
[3] C.H.Liu, et al., VLSI Tech. , pp.35-36, 2009.

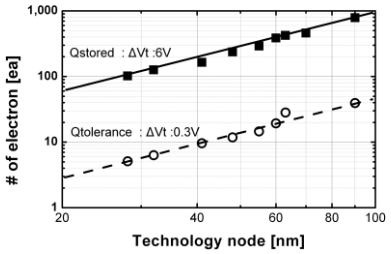

Fig.1 Stored charges and tolerance of charge loss as a function of technology node.

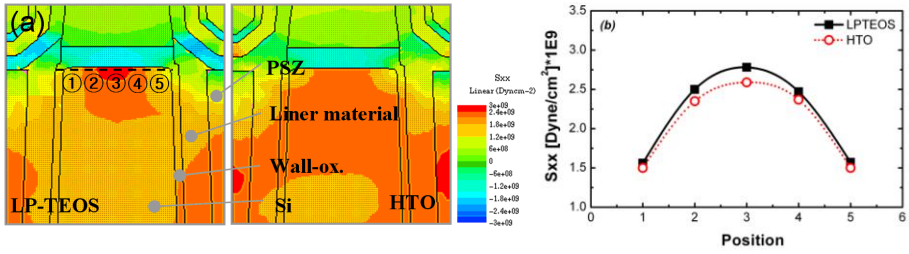

Fig.2 (a) Comparison of simulated mechanical stress between different liner materials (b) Simulated stress along channel direction depicted position in (a).

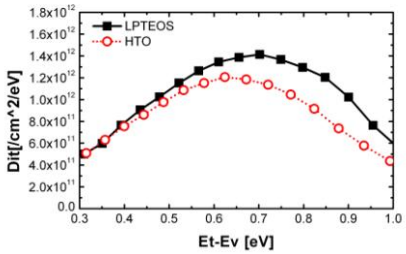

Fig.3 Comparison of interface trap density extracted between the different liner materials.

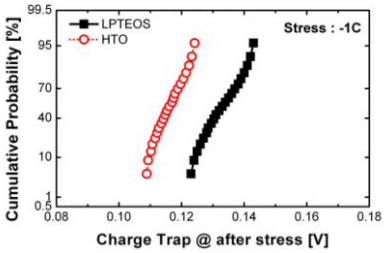

Fig.4 Comparison of charge trap as a function of voltage shift after -1C stress for STI edge intensive capacitor patterns.

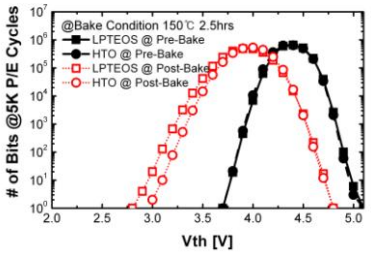

Fig.5 Cell Vth distribution after P/E Cycle with regard to different liner materials.

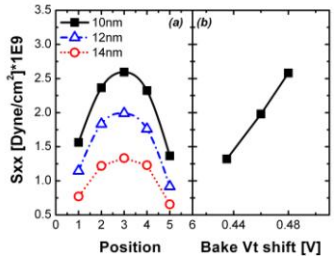

Fig.6 (a) Mechanical stress along channel as a function of liner thickness for HTO. (b) Bake shift fits shows strong correlation with the mechanical stress.

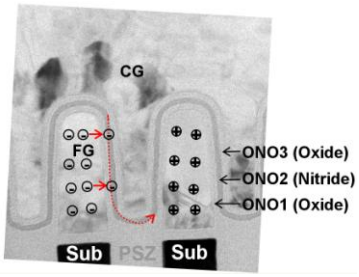

Fig.7 Possible charge loss paths through ONO stacks in Flash cell structure.

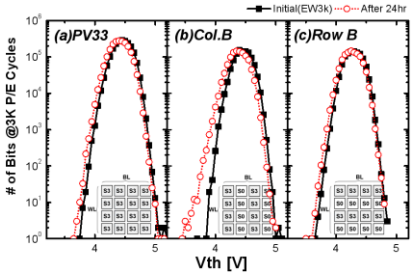

Fig.8 Cell Vth distribution with different data patterns. The depicted S0/S3 indicate different Vth states (S0≒-3V,S3≒4.0V).

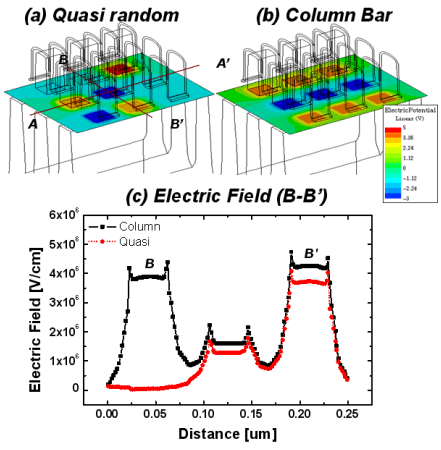

Fig.9 TCAD 3D structure to understand electric potential for various data patterns of quasi-random(a) and column bar(b). (c) Electric field along BB' lines.

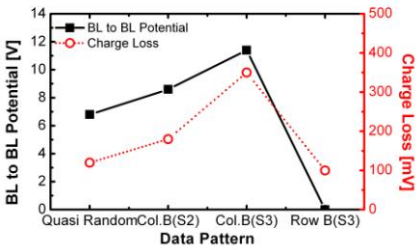

Fig.10 BL to BL potential vs. the measured charge loss (S2≒2.5V,S3≒4.0V).

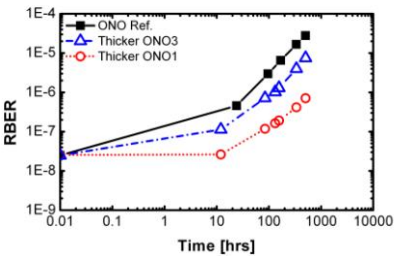

Fig.11 Data retention characteristics according to bottom and top oxide thickness trials with the same EOT.