A Low Power and Improving Read Disturb Characteristics by Using Multi-CSL Architecture in MLC NAND Flash Memory

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1. Introduction

The rapidly increasing demand on portable electronics equipments such as MP3 players, digital cameras, cellular phones, and notebook computers that require extended battery lifetime necessitates of low power operation NAND flash memory. The requirement of low power consumption which is crucial for mobile and green devices has been driving down the operating voltage of NAND flash memory [1] [2]. Also, as NAND devices are scaled down, the degradation of read disturb characteristics are an important reliability issue for future NAND flash memories [3].

To overcome power issue and improve read disturb characteristics, new operation schemes are urgently required. In this paper, we propose a new NAND string and its read operation scheme using multi-common source line (CSL) architecture to suppress power consumption and improve the read disturb characteristics. The proposed scheme was successfully demonstrated using the 40 nm NAND technology.

2. Overview of the Self-Boosting Read Scheme

Fig. 1 shows a concept of self-boosting read scheme to suppress read disturbance [3]. Also, the schematic diagram and voltage conditions of capacitive coupling model are illustrated [4]. As the coupled channel voltage rises to \( V_{cc} \), the source select line (SSL) transistor in read operation, the SSL transistor is shut off and the channel becomes a floating node. Thus, the channel voltages of unselected bitline (BL) are boosted when \( V_{\text{read}} \) voltage is applied to the unselected BL and common source line even though the channel voltage on the unselected BL, which enables that BL precharged voltage. Table 1 summarizes the read, program, and erase conditions for the proposed scheme. (\( V_{cc} \): read voltage for the selected WL, \( V_{\text{ofl}} \): read voltage for the unselected WL)

Fig. 2 shows the proposed NAND strings for multi-CSL architecture. To implement multi-CSL architecture, CSL is established by each physical and logical even/odd page and driven independently. Therefore, it is possible to apply channel voltage on the unselected BL, which enables that the channel voltages of the unselected memory cells are applied by BL and CSL and prevent F-N tunneling in the unselected memory cells. It leads to significantly improve read disturb characteristics compared with conventional scheme. As scaling NAND flash device, BL pitch also gets smaller and smaller. The BL contact should be placed in a zigzag shape from 30 nm design rule due to the difficulty in photo lithography, as shown in Fig. 3. Therefore, as NAND devices are scaled down, there is no area penalty when implementing the multi-CSL scheme. Fig. 4 shows new read bias conditions and a timing diagram. When \( V_{pc} \) is applied to the unselected BL and common source line even (CSLe), the channel voltage of the unselected NAND is precharged to \( V_{pc} \). When \( V_{\text{read}} \) is applied to the unselected WLs and ground select line (GSL), the read disturb is suppressed through multi-CSL architecture due to high precharged voltage. Table 1 summarizes the read, program, and erase conditions for the proposed scheme. (\( V_{cc} \): read voltage for the selected WL, \( V_{\text{ofl}} \): read voltage for the unselected WL)

Fig. 5 shows the measured bits in failure of read disturb at 16 Mbit test chip as a function of read cycling at \( V_{\text{read}} = 7.5 \) V. As the channel potential is increased, read disturb fail bits decreases linearly, as shown in fig. 5. The number of fail bits of proposed NAND was decreased by 56% compared to those of conventional NAND at 10³ read cycles. Also, the proposed NAND is more immune to P/E cycling at \( V_{\text{read}} = 7 \) V, as shown in fig. 6. Fig. 6 illustrates that the \( V_{\text{th}} \) shift of the proposed NAND is about 40% lower than that of the conventional NAND. SPICE simulation was performed in order to analyze the power consumption and performance. Fig. 6 shows the simulation result comparing the conventional read scheme and multi-CSL architecture with the parameters of sub-40 nm multi level cell (MLC) NAND flash memory. We have observed that BL rising time is reduced significantly due to the shielded BL to BL coupling. Moreover, the power consumption of the proposed NAND is about 70% lower than that of the conventional NAND.

4. Conclusions

We proposed a new NAND flash memory architecture and its read operation using multi-CSL architecture as a...
solution for the extremely scaled NAND flash memories. The proposed NAND flash array based on 40 nm technology were rigorously evaluated by both simulation and measurement. It was proven that they contribute to improve the performance and suppress the read disturb as well as power consumption.

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Reference