Extended Abstracts of the 2010 International Conference on Solid State Devices and Materials, Tokyo, 2010, pp752-753

Bandgap Engineered Nanowire (BEN) SONOS NAND Flash Memory

Jang-Gn Yun[1], Dae Woong Kwon[2], Jong-Ho Lee[1], Hyungcheol Shin[1], and Byung-Gook Park[1]

[1]Inter-university Semiconductor Research Center (ISRC) and School of Electrical Engineering and Computer Science, Seoul National University, San 56-1, Sillim-dong, Gwanak-gu, Seoul, 151-742, Korea
Tel: +82-2-880-7279, Fax: +82-2-882-4658, E-mail: jgyun7@snu.ac.kr
[2]Flash Process Architecture Team, Memory Division, Semiconductor Business, Samsung Electronics Co., Ltd.

1. Introduction

As the device dimension scales down, nanowire device having a gate-all-around (GAA) structure has been widely investigated to suppress the short channel effect. Besides the device performance, the GAA structure with nanowire channel is also beneficial for the NAND flash memory operation. Electric field (E-field) applied on the nanowire and tunnel oxide interface is enhanced. Also, reduced E-field on the block oxide is resulted from the field concentration effect [1],[2].

On the other hand, bandgap engineered (BE) SONOS was developed for enhancing hole tunneling efficiency during the erase operation without the degradation of data retention characteristics [3],[4]. Instead of O/N/O gate dielectrics in the SONOS, BE-SONOS uses O1/N/O2/N/O layers. The bottom O1/N/O2 layers are tunneling dielectrics in the BE-SONOS. If the O1 layer is sufficiently thin enough for direct tunneling of electrons or holes, tunneling distance becomes narrower than that of the SONOS device in which the FN tunneling is used for P/E operations.

In this paper, BE-SONOS is applied on the GAA nanowire structure to take advantages of high tunneling efficiency and field concentration effect for high speed, low power NAND flash memory application as shown in Fig. 1.

2. Fabrication Process Flow

The fabrication process flow of the bandgap engineered nanowire (BEN) SONOS memory is illustrated in Fig. 2. First, oxide and poly Si layers are deposited on a silicon-on-insulator (SOI) substrate. After patterning the active region, deposition and planarization of oxide layer is followed by gate patterning process. The damascene gate process is adopted to make the GAA structure. After dry etch of the planarized oxide and BOX, isotropic wet etch is processed to punch the exposed BOX region under the Si nanowire. Growth of O/N/O/N/O dielectrics using rapid thermal oxidation and LPCVD systems is followed by the gate material (phosphorus-doped poly Si) deposition. The gate is formed through the chemical mechanical polishing (CMP) process of the doped poly Si. For the source/drain ion implantation and activation, the planarized oxide is recessed by the plasma dry etch. The nanowire is protected from the plasma damage by the wire protection layer.

2. Results and Discussion

Fig. 3(a) shows the E-field applied on O/N/O dielectrics for both planar and GAA structures during the program operation. In case of the GAA structure, much higher E-field is applied on the tunnel oxide while E-field on the block oxide is lower than that of the planar device. When the BE-SONOS is applied on the GAA structure, the field concentration effect is still observed as shown in Fig. 3(b). Especially, the E-field across the gate dielectrics in the BEN-SONOS device is higher than that of the GAA SONOS device due to the higher dielectric constant of nitride than oxide in the tunnel dielectrics. Therefore, applied bias on the gate for the program operation can be reduced.

Moreover, program efficiency is improved in case of the BEN-SONOS device. When high program/erase voltage is applied on gate/body, tunnel oxide thickness becomes electrically thinned. The FN tunneling occurs in case of the GAA SONOS device. On the other hand, direct tunneling is possible if the BEN-SONOS device is used as shown in Fig. 4. Due to the band offset in the nitride region, tunneling width becomes narrow enough for the direct tunneling. As a result, operation speed is much faster in case of the BEN-SONOS device.

Output and transfer characteristics of the fabricated device are shown in Fig. 5. Active region is patterned by e-beam lithography for the nanowire formation (W = 70 nm). The O/N/O/N/O dielectrics of 1/2/1/6.5/6.5 are grown and deposited. Program/erase operation characteristics are shown in Fig. 6. About 3.7 V of V_{TH} window is achieved by applying ± 15 V for 10 ms. Fast program/erase speed is observed as shown in Fig. 7.

4. Conclusions

The BEN-SONOS device is introduced and fabricated for high speed, low power NAND flash memory application. Through the direct tunneling of electrons/holes by bandgap engineering of tunnel dielectrics, program/erase speed is enhanced. By applying the BE-SONOS on the GAA structure, field concentration effect can be achieved at low operation bias conditions. Program/erase properties are measured in the fabricated BEN-SONOS device showing fast transient characteristics.

References

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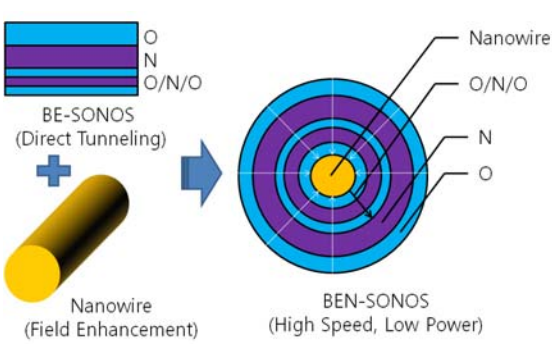
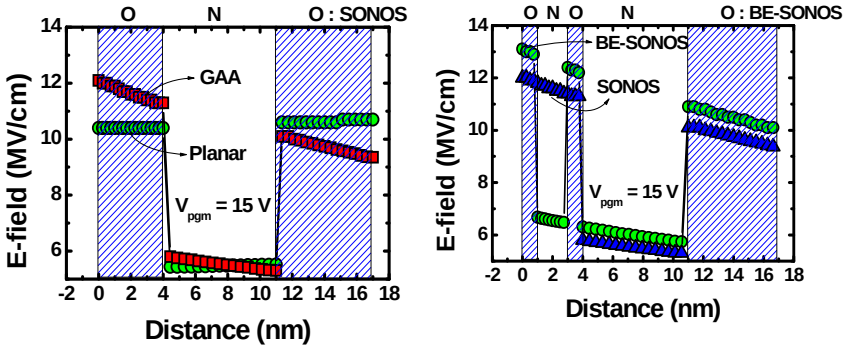


Fig. 1 Bandgap Engineered Nanowire (BEN) SONOS NAND flash memory. High speed, low power program/erase operation characteristics are resulted from 1) direct tunneling of electrons/holes by bandgap engineering and 2) enhanced field concentration effect on the cylindrical Si nanowire/tunnel oxide interface.



(a) (b)

Fig. 3 Comparison of E-field applied on O/N/O or O/N/O/N/O dielectrics during the program operation (V_{pgm} = 15 V). (a) Planar- vs. GAA-type SONOS devices and (b) GAA-type devices with O/N/O vs. O/N/O/N/O dielectrics.

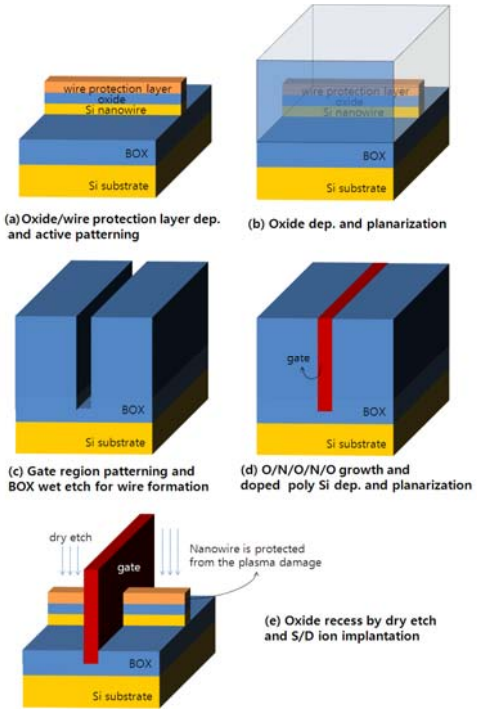


Fig. 2 Fabrication process flow of the BEN-SONOS device. Damascene gate process is used for the nanowire formation. The nanowire is protected from the plasma damage using the protection layer as illustrated in Fig. 2(e).

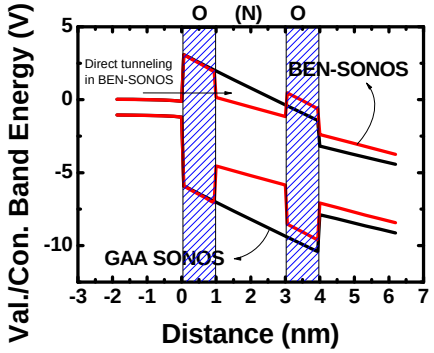
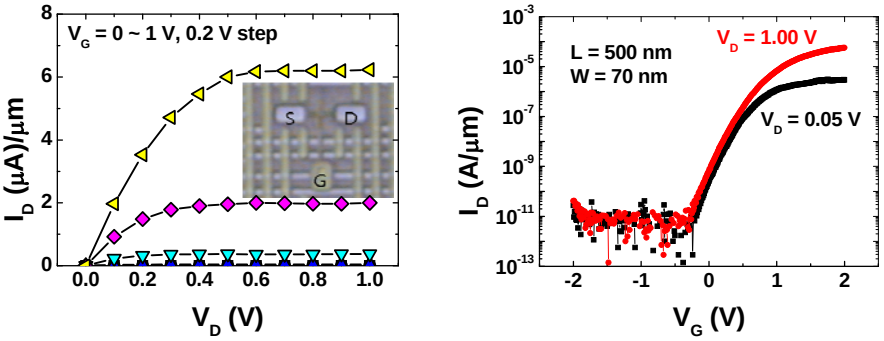


Fig. 4 Valence/Conduction band energy throughout the tunnel dielectrics in the GAA SONOS and BEN-SONOS devices. Tunneling distance is different from each other due to the band offset in the nitride region.



(a) (b)

Fig. 5 (a) Output and (b) transfer characteristics of the fabricated BEN-SONOS device (W/L = 70/500 nm). Mix-and-match process of e-beam and photo lithography is used for nanowire, gate and contact pad patterning. The nanowire regions are patterned by the e-beam lithography.

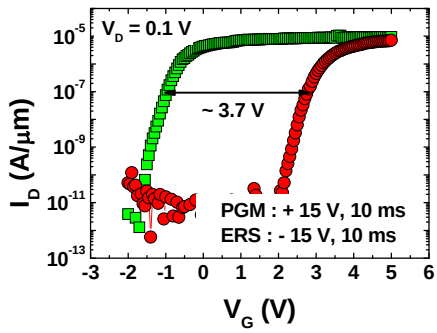
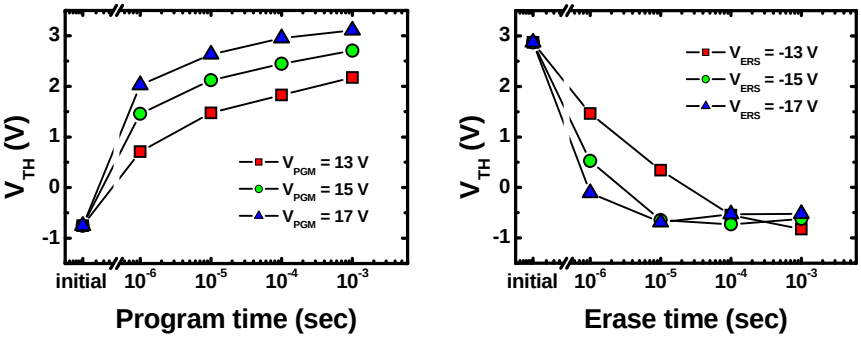


Fig. 6 Memory operation characteristics of the fabricated BEN-SONOS device.



(a) (b)

Fig. 7 Measurement results of (a) program and (b) erase speed in the BEN-SONOS device.