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Y-disturb Study of Charge-trapping Type Non-volatile Memory Cell for 45nm Generation Node

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Abstract

Neighbor word-line (WL) program disturb in a virtual ground array is studied for 45nm generation node. Unexpectedly, the interference plays no role and disturbance in the width direction (Y-disturb) is mainly induced by the injection of secondary hot electrons, which is similar to that in the length direction (X-disturb). Fine tuning the junction implantations or increasing the program WL bias can effectively improve the disturbances at both directions.

Introduction

Charge-trapping device is very attractive for replacing conventional floating gate (FG) NAND type flash memory because of slightly cell-to-cell interference beyond 40nm node [1, 2]. As demonstrated in [3], no interference is observed for a 63nm TANOS device. However, in previously study [4, 5], interference from adjacent WL has been identified in a NOR-type nitride-based flash memory even at 110nm generation node. Based on their simulations and observations, this interference effect cannot be ignored any more and should be well taken into consideration when defining the operation window for sub-60nm technologies. Predictions from NAND and NOR type arrays significantly contradicts and root causes remain unknown. In this paper, the interference effect between neighbor WLs is measured by using SONOS cells within a virtual ground NOR type array architecture [6]. In Fig. 1, threshold voltage (V_T) and punch-through voltage (V_{PT}) of cells are plotted against its mask lengths and each data is an average of 5 points. Cells with W/L=0.045/0.08 μm are chosen and the ONO stacks are 9nm/7nm/5nm.

Experimental Results

The array architecture for disturbance evaluation is schematically depicted in Fig. 2. Channel hot electron (CHE) injection is utilized for programming Bit-A from low V_T state to a high V_T state. During program, the WL bias is fixed and a stepping bit-line (BL) bias is applied until a certain V_T level is reached. The V_T state of bits nearby is also recorded and results are shown in Fig. 3. Unfortunately, none of them shows disturb free behavior. After considering these disturbances, the maximum operation window is about 2.4V. The three window killing factors are then briefly introduced as follows. Since Bit-E and Bit-A shares a same conduction path, the channel potential beneath Bit-E is unavoidable raised once electrons are stored in Bit-A. The interference for bits within a same cell is well-studied and named as 2nd bit effect [7]. Bit-B, which uses a same BL and WL with Bit-A, should be electrically isolated by the n+ junction but it suffers secondary electron injection as described in [8]. Optimizing junction implantations is helpful for this kind of disturb [9]. Similar to ref. [4, 5], Bit-C and Bit-D, which share a same BL with Bit-A but locate at neighbor WLs, are also affected by program operation. Such Y-disturb will be carefully reviewed below.

As two adjacent WLs are programmed, the V_T shift (ΔV_T) of Y-disturb becomes twice as large as one side as exhibited in Fig. 4. Moreover, in Fig. 5, the WL spacing dependence is measured. The ΔV_T becomes larger when the WLs are closer. These two properties look like consistent with the potential coupling effect, which is simulated in ref. [4, 5]. However, in Fig. 6, the Y-disturb is found to correlate with junction implantations. It is insufficient for explanation that ΔV_T is mainly contributed by capacitive coupling. Furthermore, in Fig. 7, Bit-A is firstly programmed by about 4V. Meanwhile, the V_T of Bit-C is also increased. And then, Bit-A is intentionally erased to see if Bit-C is affected or not. Unlike the interference observed in FG devices [10], the Y-disturb cannot be recovered by removing charges on Bit-A. It is thus suspected that some electrons might inject into bit-C while bit-A is programming. In other words, X and Y disturbances might both originate from the secondary electrons induced by CHE. To enhance the injection efficiency of CHE, increasing the vertical field is one of the ways. In Fig. 8, the X and Y disturbs are measured under different program WL voltage. Each data point represents an average of tens of cells when the programmed bits have a ΔV_T = 4V. As shown in the figure, both disturbances decrease with increasing program WL bias. This implies that increasing the injection efficiency of CHE can reduce the generation of excess secondary electrons. That is why fine-tuning the process implantations works as illustrated in Fig. 6. Because the X-disturb and Y disturb suffer from the same disturbance mechanism, a positive relationship should be found, as shown in Fig. 9. The correlation factor is 0.9, implying that the two disturbances indeed have a strong correlation. To further analyze these results, a 3D simulator is employed and the experimental data can be repeated qualitatively from cell current point view. In Fig. 10, the contour of surface electron current density of a simplified cell array is simulated. High gate and drain biases (V_G/V_D) are applied to emulate the program status. It is interesting to find out that the carriers not only locate at the programmed cell but also spread out to neighbor cells (Bit-B and Bit-C) in spite of the existence of n+ junctions and cell isolation implantations. In Fig. 11, three combinations of V_G and V_D are carefully chosen to keep similar injected gate current (I_G of programmed cell). Similar to Fig. 8, the gate current of disturbed cell (X-disturb and Y disturb) increased when V_G/V_D decreased. In next step, to quantitative fit the experimental results, the secondary electron energy should be considered as described in [9].

Conclusion

In this study, we find that impact ionization-generated secondary electrons not only flow to a neighbor cell (X-disturb), but also flow to neighboring WL cells (Y-disturb). Thus, the X-disturb shows a strong relationship to the Y-disturb. Higher program WL bias or process optimization can alleviate these two disturbances by enhancing CHE injection efficiency. A qualitatively analysis done by a 3D simulator is also provided.

Reference

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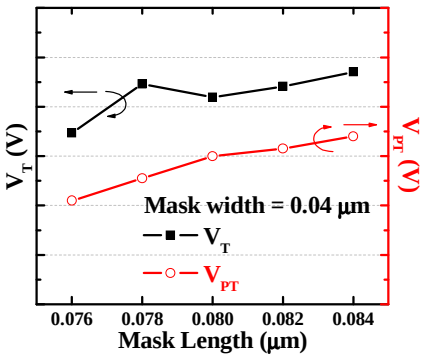

Fig.1 Threshold voltage (V_T) and punch-through voltage (V_{PT}) as a function of mask lengths.

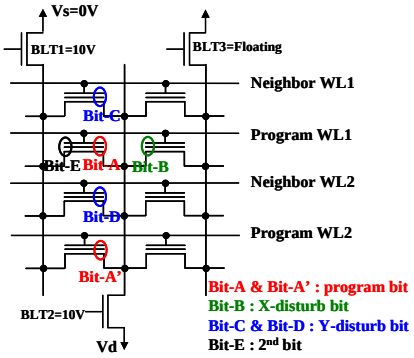

Fig.2 Schematic structure of a virtual ground mini array. Bit-A and Bit-A' are the programmed bit. Bit-B is disturbed in length direction (X-disturb). Bit-C and Bit-D are disturbed in width direction (Y-disturb). Bit-E is named as 2nd bit.

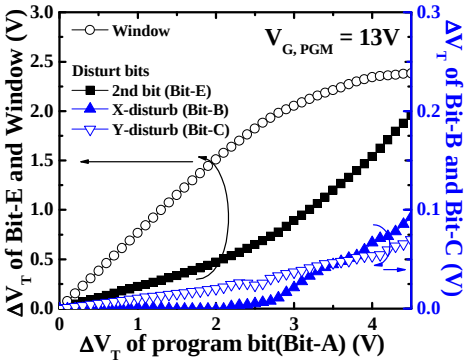

Fig.3 Left y-axis shows the window (=$V_{T,PGM}$ - $V_{T,ERS}$) and the V_T shift of the 2nd bit. Right y-axis displays the V_T shift of Bit-B and Bit-C during programming Bit-A.

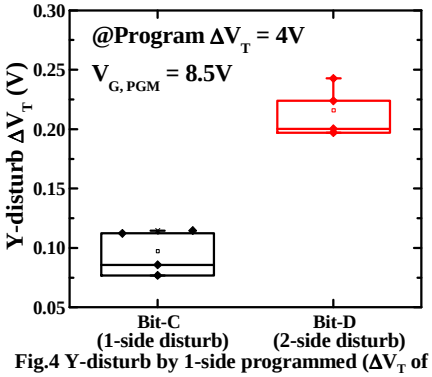

Fig.4 Y-disturb by 1-side programmed (ΔV_T of Bit-C during programming Bit-A) and 2-side programmed (ΔV_T of Bit-D when both Bit-A and Bit-A' are programmed). V_T shift of 4V in Bit-A and Bit-A' is determined.

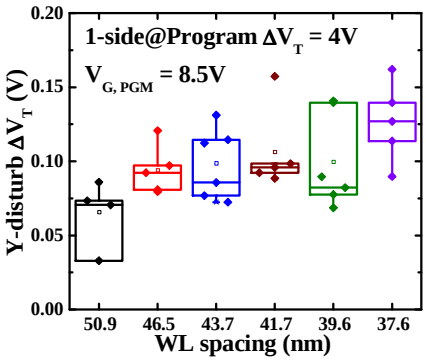

Fig.5 1-side Y-disturb for different WL spacing under 4V V_T shift in programmed bit.

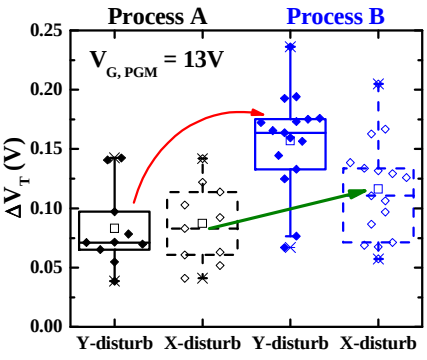

Fig.6 Optimized junction implantations (Process A) can improve Y- and X-disturb simultaneously.

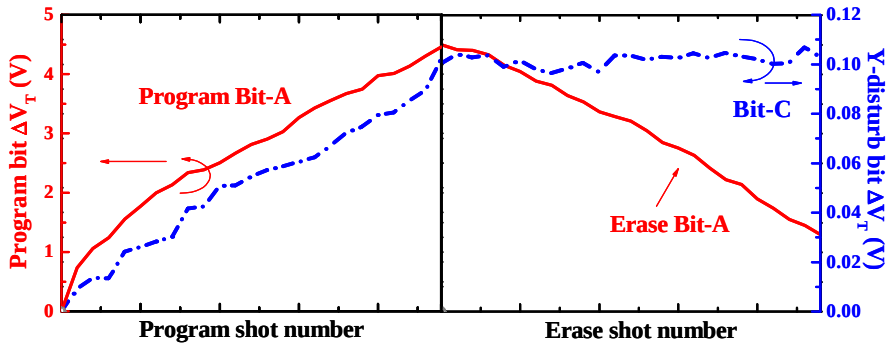

Fig.7 Program and erase transient of programmed bit (Bit-A) and disturbed bit (Bit-C). V_T shift of Bit-C increases with that of Bit-A during programming but keeps unchanged when Bit-A is erased.

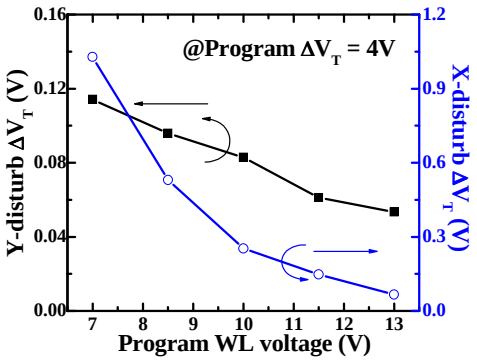

Fig.8 Program WL bias effect on Y-disturb and X-disturb. Both disturbances are suppressed with increasing WL bias.

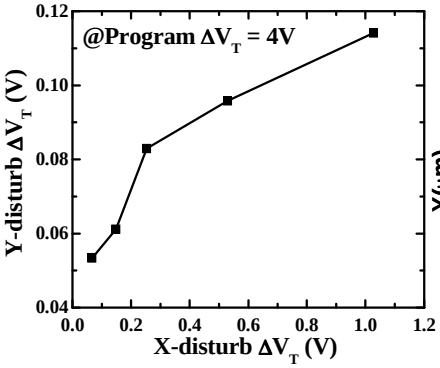

Fig.9 Y-disturb as function of X-disturb. Positive relationship is observed between these two disturbances.

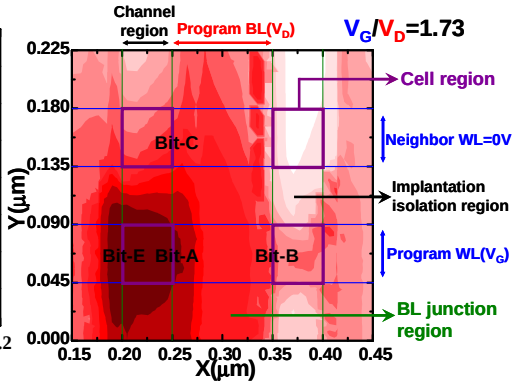

Fig.10 Surface current density simulation. Bit-A is the programmed bit. Bit-B is X-disturb bit. Bit-C is Y-disturb bit. Bit-E is 2nd bit.

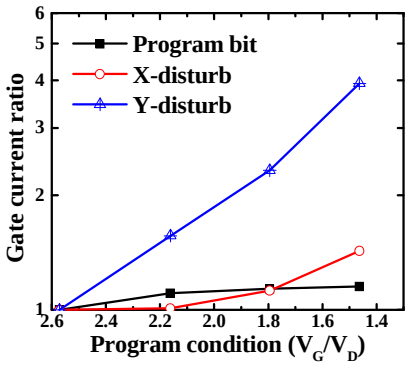

Fig.11 Gate current of disturbed cell increasing during Bit-A is programming. Each data is normalized by initial program condition.